

# 155 GHz FMCW and Stepped-Frequency Carrier OFDM Radar Sensor Transceiver IC Featuring a PLL With <30 ns Settling Time and 40 fs rms Jitter

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**Abstract**—A radar transceiver with two transmitters (TXs) and two receivers (RXs) is reported in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS. It includes a novel 200 MHz bandwidth 80 GHz phase-locked loop (PLL) based on a single-sideband (SSB) upconverter and an 11 GHz bandwidth phase-frequency detector to achieve >8 GHz locking range with record phase noise of  $-97$ ,  $-103$ , and  $-113$  dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offset, respectively, and rms jitter <40 fs. Stepped-frequency chirps with orthogonal frequency-division multiplexing (OFDM) modulation covering the 152–160 GHz range were demonstrated in a through-the-air loopback link along with a record settling time <30 ns, limited by the test equipment. The RXs have an IIP3 of  $-8$  dBm, SSB noise figure between 7.5 and 10 dB and a conversion gain of 15 dB, controllable from the LNA back gate over a range of 12 dB. The  $OP_{1dB}$  and  $P_{SAT}$  of the power amplifier (PA) in each TX are 5 and 9 dBm, respectively. The IQ amplitude mismatch and phase error of each RX are <0.5 dB and  $1^\circ$ , respectively, while the  $P_{out}$  mismatch between the TXs is <1 dB. The sensor consumes 1.13 W, with 300 mW by the PLL, 275 mW by the 160 GHz local oscillator (LO)-tree, 190 mW by each TX, and 87.5 mW by each RX.

**Index Terms**—Charge pump, D-band, divider, frequency-modulated continuous wave (FMCW), fully depleted silicon-on-insulator (FDSOI) CMOS, orthogonal frequency-division multiplexing (OFDM), phase noise (PN), phase-frequency detector (PFD), phase-locked loop (PLL), power amplifier (PA), radar, sensor, single-sideband (SSB) mixer, stepped-frequency carrier, transceiver, voltage-controlled oscillator.

## I. INTRODUCTION

STEPPED-FREQUENCY [1], [2] and linear frequency-modulated continuous wave (FMCW) [3] orthogonal

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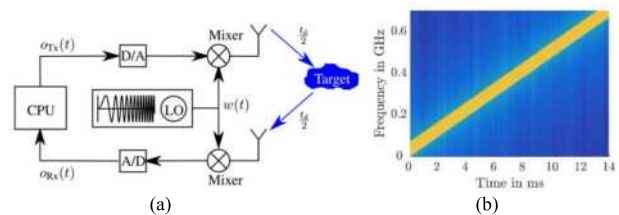


Fig. 1. OFDM radar sensor concept with linear FMCW carrier. (a) Block diagram and (b) linear FMCW chirp with OFDM modulation highlighting the <50 MHz occupied bandwidth (yellow stripe) as a function of time [3].

frequency-division multiplexing (OFDM)-based multiple-input and multiple-output (MIMO) radar networks have been proposed recently for next-generation radar sensors to reduce interference and significantly improve distance, velocity, and angle resolution [4]. The concepts of low (<100 MHz) IF-bandwidth,  $B_{IF}$ , OFDM modulation superimposed on top of a linear FMCW carrier, or on a stepped-frequency carrier, are illustrated in Figs. 1 and 2, respectively, and were demonstrated using discrete components at 24 GHz [3] and 75 GHz [2], respectively. As depicted in Fig. 1(a), in order to benefit from the reduced IF bandwidth, the frequency step or ramp have to be formed in the local oscillator (LO) path of the system while the OFDM modulation signal must be generated with a separate digital-to-analog converter (DAC). The OFDM modulation is then linearly upconverted and synchronized with the linear ramp or frequency step [2]. Both concepts allow for a wide (>8 GHz) radar modulation bandwidth,  $B_{mod}$ , to be covered without the need for multi-GS/s analog-to-digital converters (ADCs) and DACs.

In the first type of radar system, low phase noise (PN) and a flexible, linear, and precise ramp (chirp) are required from the LO signal generator [3]. For the second, in addition to low PN, short and precise frequency steps, with duration,  $T_{step}$ , smaller than  $4 \mu s$  and settling time  $\ll 4 \mu s$ , are needed [2]. The relationship between the IF bandwidth and the modulation bandwidth is given by  $B_{mod} = S_b \times B_{IF}$ , where  $S_b$  represents the number of frequency steps. The frequency step size is  $N_C \times \Delta f_c$ , with  $N_C$  and  $\Delta f_c$  being the number of OFDM subcarriers and the subcarrier frequency spacing, respectively, as shown in Fig. 2(b).

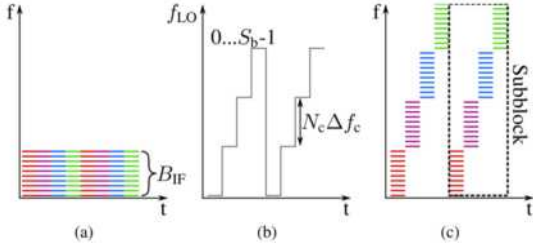


Fig. 2. Modulation structure of stepped-carrier OFDM radar where  $S_b$  is the number of steps,  $N_c$  is the number of subcarriers, and  $\Delta f_c$  is the subcarrier spacing. (a) Instantaneous signal bandwidth,  $B_{IF}$ , at the TX input and RX output, (b) instantaneous LO signal frequency,  $f_{LO}$ , and (c) symbols at the RF TX output consisting of several subcarriers illustrating the instantaneous RF bandwidth [2].

Comparing the two modulations schemes, the stepped-carrier variant is more interesting for automotive applications as the stepping allows flexible modulation design, with the degrees of freedom provided by  $N_c$ ,  $S_b$ , and the number of symbols,  $M_s$  [2]. The carrier generation, however, imposes high demands on timing and frequency accuracy which calls for an ultralow noise and fast-settling phase-locked loop (PLL) with  $<100$  ns settling time which has never been realized before. To circumvent the latter problem, the stepped-frequency carrier OFDM sensor in [2] was realized with discrete components, combining two voltage-controlled oscillators (VCOs), two PLLs, and a fast switch with nanosecond-scale dead time. To generate the stepped-frequency carrier with reduced frequency step overshoot, only one VCO was switched to the LO generator output while the second VCO had  $4 \mu s$  to settle before it was connected to the LO output. This scheme is expensive in terms of components and significantly increases power consumption.

As indicated above, PN is a key performance figure for all radar sensors, irrespective of modulation format. For single-sensor short-range operation, the autocorrelation of the oscillator signal may suppress PN to an acceptable level. For longer travel times (higher distance) this effect diminishes and, when working with multiple radar sensor chips [5], low PN becomes crucial if no central FMCW LO source can be used to synchronize them [5], [6]. In cooperative multiple sensor networks aiming for high angle resolution [6], [7], a low PN of  $<-77$  dBc/Hz at 10 kHz offset and  $<-97$  dBc/Hz at 100 kHz is required to enable bistatic or multistatic operation [7]. Best-in-class 77 GHz FMCW radar VCOs show PN of about  $-80$  dBc/Hz at 100 kHz offset and use SiGe HBT technology because of its low  $1/f$  noise corner. When inserted into an offset PLL with 2 MHz loop bandwidth and 167 GHz crystal reference, record low PN values of  $-97$  and  $-98$  dBc/Hz were measured at 10 and 100 kHz offset, but the  $-94$  dBc/Hz value at 1 MHz offset [7] remains too high for the desired rms phase error  $<1^\circ$ .

Unfortunately, at D-band (110–170 GHz) PN worsens as the noise figure and gain of active components degrade and interconnect losses increase, making low PN transceiver design even more challenging. For example, the architecture of the individual 160 GHz FMCW transceiver monolithic microwave

integrated circuit (MMIC) [9] used in the MIMO sensor array reported in [5] was optimized for low PN operation with a combination of multiplication and linear up-conversion outside the integer- $N$  PLL used to generate the LO signal. The low-PN, 8–12 GHz ramp signal was realized with an off-the-shelf fractional PLL and an external low-PN, wideband VCO. A PN of  $-82$  and  $-87$  dBc/Hz was measured at 100 kHz and 1 MHz offsets, respectively [5]. These values are comparable to those of the D-band sensor in [10], which uses the same 80 GHz PLL as [8], but significantly higher than the theoretical 6 dB when compared with those reported for the 80 GHz PLL in [8].

In this article, we report the first fully integrated radar sensor transceiver which can accommodate classical FMCW, linear FMCW OFDM, and ultra-fast stepped-frequency carrier OFDM radar modulation schemes. This enhanced functionality is enabled by a novel on-die 80 GHz PLL with record low PN and settling time, lower than 30 ns, enabling 100 ns frequency steps,  $40\times$  smaller than in [2]. Fast ( $<1 \mu s$ ) FMCW and stepped-frequency OFDM chirps are needed for spectral sensing in interference-aware collaborative radar networks [11] but have not been demonstrated before.

The radar sensor transceiver was manufactured in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology. It features dual-channel operation for polarimetric measurements, operates in the 160 GHz band for high-velocity resolution taking advantage of the small wavelength, and allows 8 GHz of modulation bandwidth for high distance resolution. The ultralow PN, at least 10 dB better than the state-of-the-art D-band, and the digital modulation enable bistatic operation with two or more sensors in a distributed MIMO sensor network in order to obtain high-resolution angle information [4]. The breakout of the 80 GHz PLL also demonstrates at least 6 dB lower PN than that of all other 77 GHz automotive radar PLLs in SiGe BiCMOS and CMOS technologies to date.

This article is organized as follows. Section II describes the D-band sensor architecture and design specification. The choice of PLL architecture, PN model, design methodology, and transistor-level building-block schematics are covered in Section III. This is followed by the transistor-level schematics and design of the dual-channel IQ transceiver in Section IV. Section V presents the on-die transceiver characterization. The significance of this work and a comparison with the state of the art are discussed in conclusion.

## II. RADAR SENSOR ARCHITECTURE

Fig. 3 shows the block diagram of the manufactured 22 nm FDSOI dual-channel radar sensor transceiver which operates from 0.8-, 1.6-, and 2.4 V power supplies. It consists of: 1) two variable output power transmitters (TXs) and two variable gain receivers (RXs) intended to drive off-chip vertically and horizontally polarized antennas, respectively; 2) a fast-settling 80 GHz PLL with 10 GHz reference and low-frequency linear or stepped-frequency chirp IQ inputs; 3) a frequency doubler; and 4) a single-ended 160 GHz LO distribution tree that drives the two IQ downconvert- and two IQ upconvert mixers. IQ phase and amplitude error controls are provided for the upconvert and downconvert mixer pairs in the  $90^\circ$  hybrid

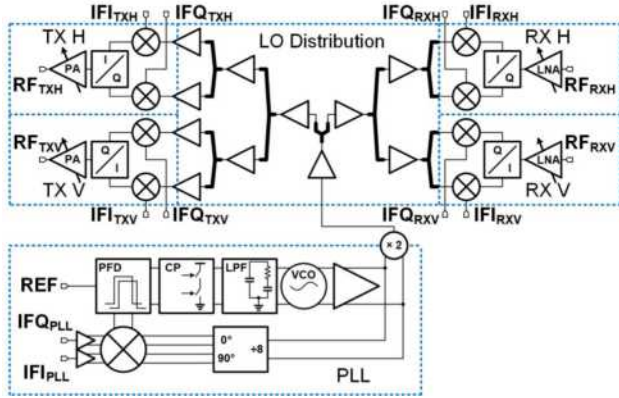


Fig. 3. Block diagram of the D-band dual-channel IQ radar sensor transceiver with integrated PLL.

couplers (symbols with  $I/Q$  label) placed on the RF paths of each TX and RX between the LNA and the downconvert mixers, and between the upconvert mixers and the power amplifier (PA). This scheme with in-phase LO and quadrature RF-path signal splitting and combining is easier to implement with lower power consumption, smaller footprint and better RX and TX linearity at 160 GHz than the alternative approach with quadrature LO signals and in-phase RF signals. To avoid more complicated and larger footprint differential  $90^\circ$  hybrids and to simplify testing at D-band, the LNA and the PA use single-ended topologies while the receive and transmit mixers are fully differential to improve image rejection and reduce LO leakage. The physical distance between RX channels must be small to allow feeding a polarimetric antenna.

As mentioned previously, to relax the IF DAC and IF ADC bandwidth requirements, the OFDM modulation is applied at the TX IF inputs while the stepped frequency or FMCW carrier chirp is formed within the LO generator. The typical OFDM modulation bandwidth of interest for the envisioned radar application is 50–150 MHz [1]. There are three external signal sources (IFPLL, IFTX, and REF) needed to realize the radar signal and all three contribute to the output PN. The noise contribution of the REF and IFPLL sources is minimized by the choice of PLL architecture and design. Since the IFTX signal is directly upconverted to 155 GHz and its bandwidth is less than 150 MHz, its PN can be easily made negligible, even if a DAC with moderate output noise is used to generate it. The DACs and ADCs are not integrated on this chip. Commercial arbitrary waveform generators (AWGs) and a real time oscilloscope (RTOS) are used instead for testing to demonstrate the unique transceiver functionality. All 160 GHz inputs and outputs, 10 GHz and IF PLL inputs, and TX IF inputs are matched to  $50 \Omega$ . The IF outputs of the two RXs have  $350 \Omega$  impedance.

The transceiver design specification parameters to accommodate both linear FMCW and stepped-frequency carrier OFDM modulation are summarized in Table I using the equations presented in [1]–[3]. This transceiver performance is also achievable in an advanced SiGe BiCMOS technology. Because of the large PLL bandwidth, the  $1/f$  noise corner

TABLE I  
TRANSCIEVER DESIGN SPECIFICATION

Description	Parameter	Value
Fundamental frequency	$f_0$	155 GHz
RF modulation bandwidth	$B_{MOD}$	8 GHz
IF bandwidth	$B_{IF}$	> 100 MHz
OFDM subcarrier spacing	$\Delta f_c$	> 200 KHz
LO frequency step	$T_{step}$	< 400 ns
PLL settling time	$T_{settling}$	< 40 ns
Ramp duration	$T_{mod}$	1–100 $\mu$ s
Linear ramp slope	$k_r$	0.08– 8 GHz/ $\mu$ s
PLL reference	$f_{REF}$	8.5–11 GHz
PLL IF input frequency range	PLL-IQ $B_W$	<1.6 GHz
PLL IF input linear voltage range	PLL-IQ $P_{1dB}$	> -10 dBm
rms phase error (100 Hz–100 MHz)	PLL-PE	< $1^\circ$
80-GHz VCO+buffer phase noise	PN @ 10 MHz	<-110 dBc/Hz
	PN @ 100 MHz	<-130 dBc/Hz
Receiver noise figure	NF	<12 dB
Receiver gain	Rx Gain	> 15 dB
Receiver linearity	IIP3	> -20 dBm
Transmitter output power	$P_{outdB}$	> 4 dBm
Power dissipation	$P_{DC}$	< 1.2 W

of the VCO PN characteristics, a weakness of all CMOS technologies, is not as critical as in other radar sensor systems. The 22 nm FDSOI CMOS technology was chosen because of its unique series-stacking and back-gate voltage performance tuning which leads to simpler circuit topologies than in other CMOS or SiGe BiCMOS technologies and to excellent performance at D-Band, comparable to that of advanced SiGe BiCMOS technologies, while consuming less power. It also allows for higher density, lower voltage and power, and faster 0.8 V CML and CMOS gates, critical for the 80 GHz PLL, than those possible in older CMOS technologies.

### III. PLL DESIGN

In W-Band [2], [8] and D-Band [5]–[7], [9], [10] radar sensors, LO generators are realized using multiplication or a combination of mixing and multiplication of a frequency ramp generator and of lower frequency ultralow PN crystal, surface acoustic wave (SAW), and dielectric resonator oscillators (DROs). The choice of multiplication factor is dictated by PN and loop stability. In general, a lower multiplication factor leads to both lower PN and more flexibility in the design of a stable loop. Assuming that the phase-frequency detector (PFD), charge pump, loop filter, and divider can be designed to have negligible PN contributions (a big ask), the PN at the PLL output is limited by the PN of the reference oscillator and of the ramp generator. It is therefore important to choose a reference oscillator whose PN contribution to the 155 GHz output of the TX is as low as possible. In [5], a 916 MHz SAW oscillator reference was used with a PN of  $-150$  dBc/Hz at 100 kHz offset, a value which could not be achieved by multiplication from a 100 MHz or lower frequency crystal reference. This PN scales to  $-105.4$  dBc/Hz at 155 GHz and sets the best achievable in-band PN. However, a 916 MHz reference limits the maximum loop bandwidth to about 18 MHz, which is not sufficient to satisfy the <40 ns settling time specification of the proposed sensor.

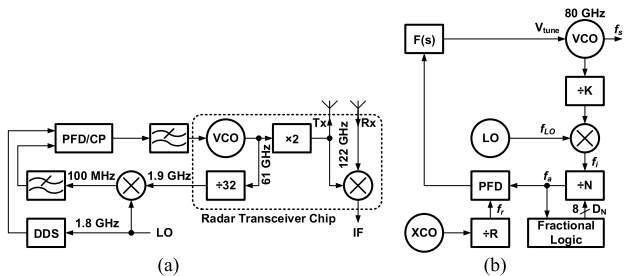


Fig. 4. Block diagrams of (a) 120 GHz integer- $N$  [7] and (b) 80 GHz fractional- $N$  [8] offset-PLL.

Unlike multiplication which amplifies it, mixing preserves PN and, when used inside the PLL, also reduces the multiplication factor, thus simplifying loop stability design. These properties of mixing are exploited in offset PLLs, which employ a double-sideband (DSB) downconversion mixer [7], [8], as shown in Fig. 4. The divider chain can be placed entirely before [7], Fig. 4(a), or after the mixer, or partly before and partly after the mixer [8], as shown in Fig. 4(b). To date, offset PLLs have demonstrated the lowest PN in radar sensors above 70 GHz. The penalty is the need for a second ultralow PN oscillator or PLL to provide the LO signal to the mixer. In [8],  $f_{\text{REF}} = 167$  MHz and  $f_{\text{LO}} = 48$  GHz, with the latter obtained using a second mm-wave PLL and a second reference SAW oscillator at 1 GHz, as in [5]. The total multiplication factor seen by the reference and ramp signals is still large,  $N \times K = 24$ –168, where  $K = 2$ , and  $N$  varies between 12 and 84. In both [7] and [8], the LO signal is used to derive the sampling clock for the direct digital synthesizer (DDS) which generates the ramp signal. To avoid a second reference oscillator, in [7], the PFD reference signal is derived from the 1.8 GHz LO which also drives the mixer. The LO signal itself is obtained by multiplication of a 100 MHz crystal reference [7]. The loop multiplication factor of 32 seen by the ramp and reference signals remains large. After the 61 GHz doubler, the measured PN at 122 GHz was  $-85$  dBc/Hz at 1 MHz offset and remained  $< -80$  dBc/Hz in the 300 kHz loop passband down to 2 kHz, dominated by VCO, PFD, DDS, and loop filter noise. The measured scaled PN contribution of the 1.8 GHz LO to the 122 GHz output PN was  $-95$  dBc/Hz in the passband and  $-103$  dBc/Hz at 1 MHz offset, 15 dB lower than the PLL output PN, and thus negligible.

To reduce the impact of the PN contribution of the ramp generator, in [5] and [9] the external 8–12 GHz FMCW ramp signal was not inserted in the PLL. Instead, it was fed to an on-die  $\times 4$  multiplier whose 32–48 GHz output was mixed with that of the 117 Hz fixed-frequency on-die integer-PLL LO and upconverted to 149–165 GHz. The reference signal of the PLL was provided by the 916 MHz SAW oscillator mentioned previously. The ramp source and the integer-PLL LO contributed equally to the PN of  $-87$  dBc/Hz at 1 MHz offset measured at the 160 GHz TX output.

Finally, in yet another approach to reduce its PN contribution, in [12], the linear FMCW ramp was generated using a low-noise capacitive QDAC and applied at the high-pass transfer node of the loop, directly to the 9–10.2 GHz VCO.

The measured PN was  $-109$  dBc/Hz at 1 MHz offset. This value scales to  $-83$  dBc/Hz after multiplication by 16–152 GHz and is higher than the values measured in [5] and [10]. It suggests that multiplication from a lower frequency CMOS PLL might not provide better PN at 160 GHz.

Based on the discussion above, a state-of-the-art 10 GHz DRO with a PN of  $-127$  dBc/Hz at 100 kHz [13] was chosen as the reference for the proposed 80 GHz PLL. Although any reference frequency higher than 4 GHz would satisfy the PLL settling time requirements, this DRO performance scales to the lowest possible PN value at 155 GHz of  $-103$  dBc/Hz at 100 kHz offset and results in a loop multiplication factor,  $N$ , of only 8. The envisioned approach is therefore to use this low-PN DRO as the PLL reference and a high-speed PFD to lock the millimeter-wave VCO. However, the design of an 11 GHz PFD in CMOS poses significant challenges. To the best of the authors' knowledge, the fastest reported to date operates at 5 GHz and uses SiGe BiCMOS CML logic [14].

Since the DRO frequency is fixed, an additional single sideband (SSB) upconvert mixer is added to the PLL in order to enable linear- or stepped-frequency modulation of the carrier. An IQ signal, obtained from an external DAC, DDS, or AWG, applied at the IF inputs of the mixer and a large-bandwidth PLL loop filter will then enable fast modulation speeds and the desired functionality. The block diagram of the proposed third-order PLL is included in Fig. 3. It features an 11 GHz bandwidth PFD and charge pump, the fastest to date, a passive  $R$ - $C$  differential second-order low-pass filter, a fundamental frequency 80 GHz VCO with output amplifier followed by a static divide-by-8 chain which provides precise process, supply, and temperature insensitive quadrature clock signals to a SSB linear upconvert mixer. The low frequency IQ inputs of the mixer must be in the 300–1600 MHz range, above the loop filter bandwidth, the higher the better, to attenuate spurs resultant from imperfect image rejection in the SSB mixer.

This architecture differs from that of a traditional offset-PLL [7], [8], [10] in two important aspects. First, it does not require a second LO and reference source to drive the mixer, thus saving power consumption and external components. The LO signal is provided for free by the quadrature outputs of the divider in the loop. Second, an SSB upconvert rather than a DSB downconvert mixer is used in the loop. Upconversion from a low IF frequency relaxes the noise specification and design of the ramp generator. The challenge is posed by the design of the SSB mixer with excellent image and LO leakage suppression and of a fast PFD and charge pump capable of processing the 8.5–11 GHz reference oscillator and SSB mixer output signals.

#### A. Phase Noise Analysis and Loop Bandwidth Design

The PN model of the proposed PLL is illustrated in Fig. 5(a) and bears striking resemblance to that of the offset PLL in Fig. 5(b). As in the case of the DSB downconvert mixer in Fig. 5(b), the SSB upconvert mixer is represented by its phase domain transfer function,  $K_{\text{mix}}$ , which is equal to 1 since the phases of the IFPLL IQ input and of the quadrature clock signals from the divider output are simply

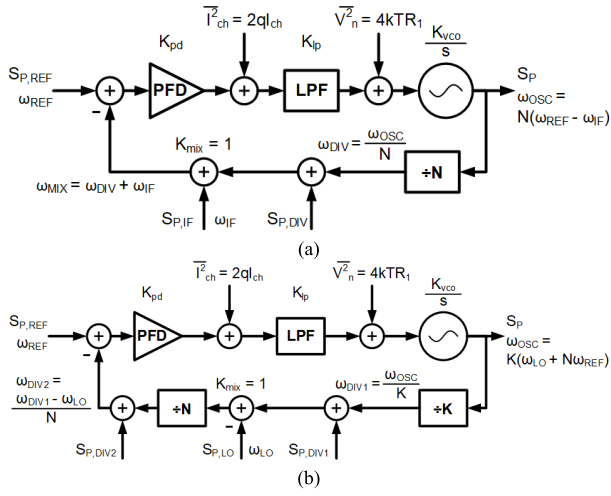


Fig. 5. PN model of (a) proposed PLL compared to (b) the 80 GHz fractional- $N$  offset-PLL in [8] and [10].

transferred to the mixer output

$$V_{O_{\text{mix}}}(t) = A \cos[(\omega_{\text{div}} \pm \omega_{\text{IF}})t + \varphi_{\text{IF}} + \varphi_{\text{div}}]. \quad (1)$$

The PLL output frequency,  $\omega_{\text{OSC}}$ , is given by (2) while the expressions of the jitter (noise) transfer functions from the DRO reference input,  $H_{\text{REF}}$ , and from the IQ SSB mixer input,  $H_{\text{IF}}$ , to the 80 GHz VCO output are identical, given by (3)

$$\omega_{\text{OSC}} = N(\omega_{\text{REF}} \pm \omega_{\text{IF}}) \quad (2)$$

$$H_{\text{REF,IF}}(s) = N \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{\text{PLL}}^2}} \quad (3)$$

where  $N$  is the divider ratio,  $\omega_z$  and  $\omega_{\text{PLL}} = (K_{\text{pd}}K_{\text{lp}}K_{\text{vco}}/N)^{1/2}$  are the 0 and PLL characteristic angular frequencies, respectively. Similarly, the expressions of the output frequency and of the jitter transfer function for the reference/ramp and LO of the 80 GHz offset PLL in [8] are given by (4), (5), and (6), respectively,

$$\omega_{\text{OSC}} = N(\omega_{\text{LO}} - K \times \omega_{\text{REF}}) \quad (4)$$

$$H_{\text{REF}}(s) = K \times N \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{\text{PLL}}^2}} \quad (5)$$

$$H_{\text{LO}}(s) = K \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{\text{PLL}}^2}}. \quad (6)$$

Equation (2) shows that, even if the reference frequency is fixed,  $\omega_{\text{OSC}}$  can be tuned over a wide frequency range by changing the frequency of the IF input signal to the SSB mixer. For example, with  $f_{\text{REF}} = 9.25$  GHz, by sweeping the frequency of a sinusoidal signal applied to the IF-PLL inputs from 500 MHz to 1 GHz, the PLL output frequency varies between 78 and 82 GHz. The  $\pm$  sign (i.e., selecting the upper or lower sidebands at the output of the mixer) can be flipped by swapping the phase of the  $I$  and  $Q$  IF inputs of the SSB mixer. This means that any DRO in the 8.4–11.1 GHz range can be used as reference oscillator to cover the desired PLL output tuning range of 76–80 GHz. Significantly, (3) indicates

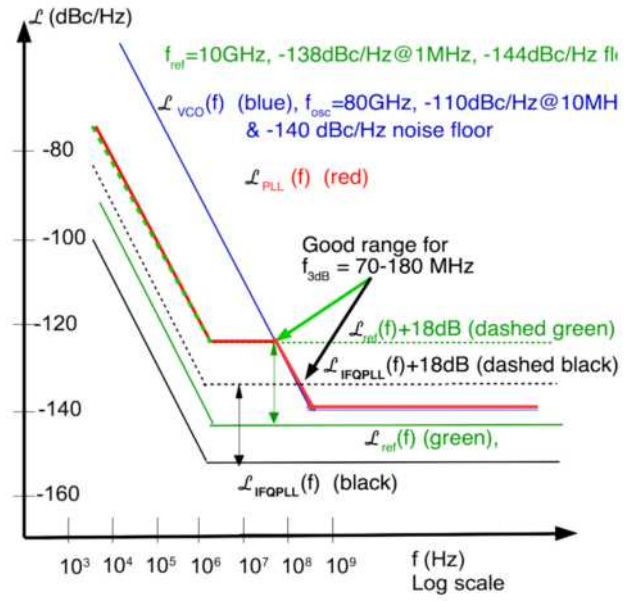


Fig. 6. Graphical method for choosing the PLL bandwidth to minimize rms phase error for scenarios when the PN of the reference dominates (green) or when the ramp generator PN dominates.

that the contributions to the PLL output PN due to the DRO PN and due to the PN at the IFPLL input are identical and follow a low-pass filter transfer function. Since the reference oscillator frequency is typically  $10\times$  higher, the PN of the ramp signal source at the IF input of the PLL can presumably be made 10 dB lower and thus its contribution rendered negligible compared to that of the reference.

To minimize the integrated jitter, the PLL bandwidth is chosen as the crossover offset frequency where the sum of the PN of the reference oscillator and of the IF ramp signal multiplied by  $N$  is equal to the PN of the free running 80 GHz VCO. This graphical design method is illustrated in Fig. 6 for the scenario with negligible PN at the IF input of the PLL and with the commercial E8527D signal source as the 10 GHz reference oscillator. The latter has  $-118$  and  $-138$  dBc/Hz PN at 100 kHz and 1 MHz offsets, and a thermal noise floor of  $-144$  dBc/Hz. In this case, the best choice loop bandwidth is 70 MHz, resulting in an integrated phase error from 1 kHz to 1 GHz of  $0.4^\circ$ . If the 10 GHz DRO in [13] with a noise floor of  $-170$  dBc/Hz above 10 MHz offset, as shown in Fig. 7, is used as reference, then the best loop bandwidth to minimize the PLL PN goes to infinity. In practice, it will be determined by the PN of the IF ramp signal source whose noise was neglected in this simple example. If we assume that the ramp generator noise floor is  $-153$  dBc/Hz as in [8], the intercept of the VCO PN plot with the upconverted  $-135$  dBc/Hz noise floor of the ramp occurs at 178 MHz. Both scenarios are captured in Fig. 6.

By making the charge pump current adjustable, the 3 dB bandwidth of the PLL can be tuned between 50 and 300 MHz, which satisfies the fast-settling requirements. It also accommodates the higher PN (by  $>10$  dB compared to that of [13]) of

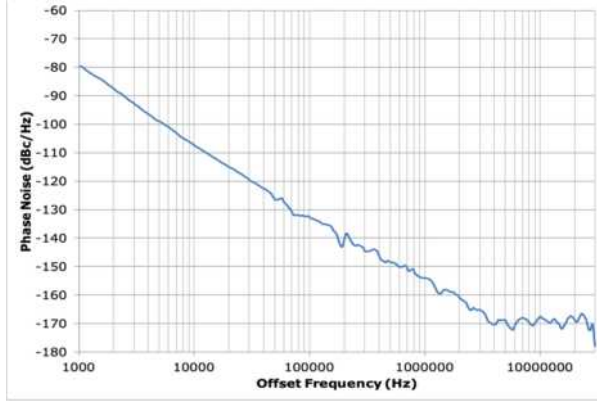


Fig. 7. Measured 10 GHz DRO PN [13].

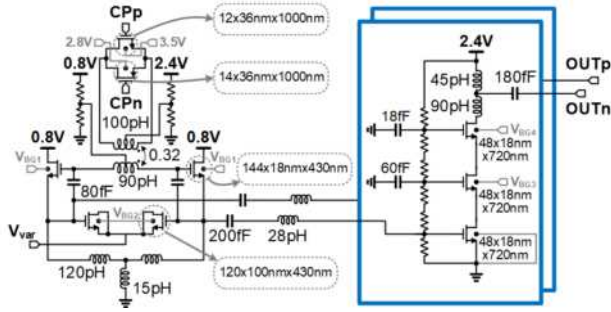


Fig. 8. Schematic of the 80 GHz VCO with large-swing output buffer.

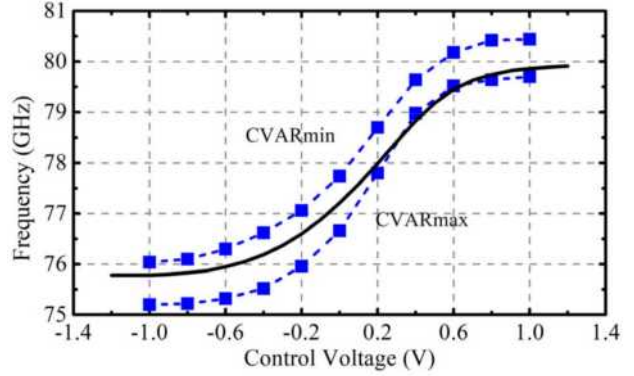
the reference signal source and AWG used in the laboratory for on-die testing of the sensor transceiver.

The transistor-level design and schematics of some of the more critical PLL blocks are discussed next. Most of the PLL blocks operate with a 0.8 V supply drawing 262 mA, except for the charge pump and the 80 GHz output buffer which are biased from 2.4 V and draw a total of 25 mA.

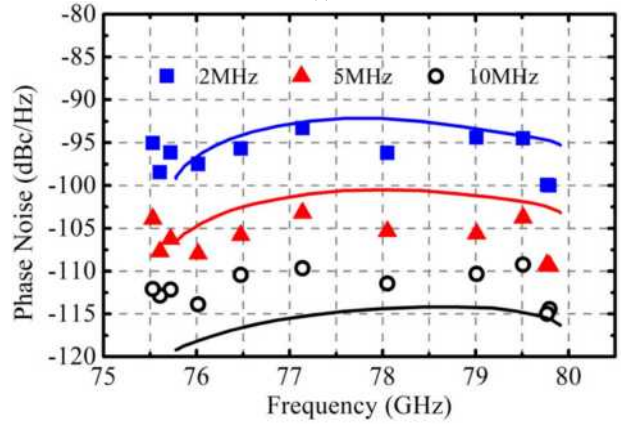
### B. Inductively Tuned Colpitts 80 GHz VCO

The VCO, depicted in Fig. 8, employs a modified differential Colpitts topology with dual varactor (single-ended coarse) and variable inductor (differential fine) tuning. The latter function is based on the resistively tuned inductor concept proposed in [15] and is realized with a transformer whose primary acts as the VCO differential tank inductance and with the secondary terminated on a novel variable resistor with differential control formed with a matched ( $K_p = K_n = K$ ) parallel-connected n-/p-MOSFET pair operating in the triode region at  $V_{DS} = 0$ . Ignoring MOSFET parasitic capacitances, the expressions of the variable tank inductance,  $L_{\text{tank}}$ , and resistance,  $R_{\text{tank}}$ , of the primary due to the variable resistance in the transformer secondary,  $R_{\text{var}}$ , become

$$L_{\text{tank}} = L_1 - \frac{L_2}{\left(\frac{L_2}{M}\right)^2 + \left(\frac{R_{\text{var}}}{\omega M}\right)^2} \text{ and } R_{\text{tank}} = \frac{R_{\text{var}}}{\left(\frac{L_2}{M}\right)^2 + \left(\frac{R_{\text{var}}}{\omega M}\right)^2} \quad (7)$$



(a)



(b)

Fig. 9. (a) Measured (dashed lines with symbols) VCO breakout tuning range versus differential control voltage for the extreme settings of the coarse control voltage compared to simulated center control voltage (solid line). (b) Measured (symbols) versus simulated (lines) VCO breakout PN.

where

$$1/R_{\text{var}} = K(V_{\text{CPp}} - V_{\text{CPn}} + V_{\text{tp}} - V_{\text{tn}}). \quad (8)$$

$L_1$ ,  $L_2$ , and  $M$  are the transformer self and mutual inductances, and  $V_{\text{tn}}$  and  $V_{\text{tp}}$  are the n-/p-MOSFET threshold voltages.

This differential control scheme allows for its common-mode dc voltage to be decoupled from that of the VCO core and thus accommodate the optimal charge-pump output voltage swing while keeping a low VCO supply of 0.8 V. The Colpitts topology was preferred to the cross-coupled one in [16] because of its better PN for a given tuning range.

To minimize the PN, the VCO supply is separated and isolated from the rest of the PLL using wide, grounded substrate stripes. The VCO consumes a relatively large current of 36 mA to reduce PN while achieving >8% tuning range (coarse and fine). The simulated and measured VCO-with-buffer performance is illustrated in Fig. 9(a) as a function of the differential tuning voltage of the variable resistor. PN peaks at  $-93$  dBc/Hz at 2 MHz offset in the center of the simulated tuning range where the noise contributions from the transformer and variable resistor are highest and

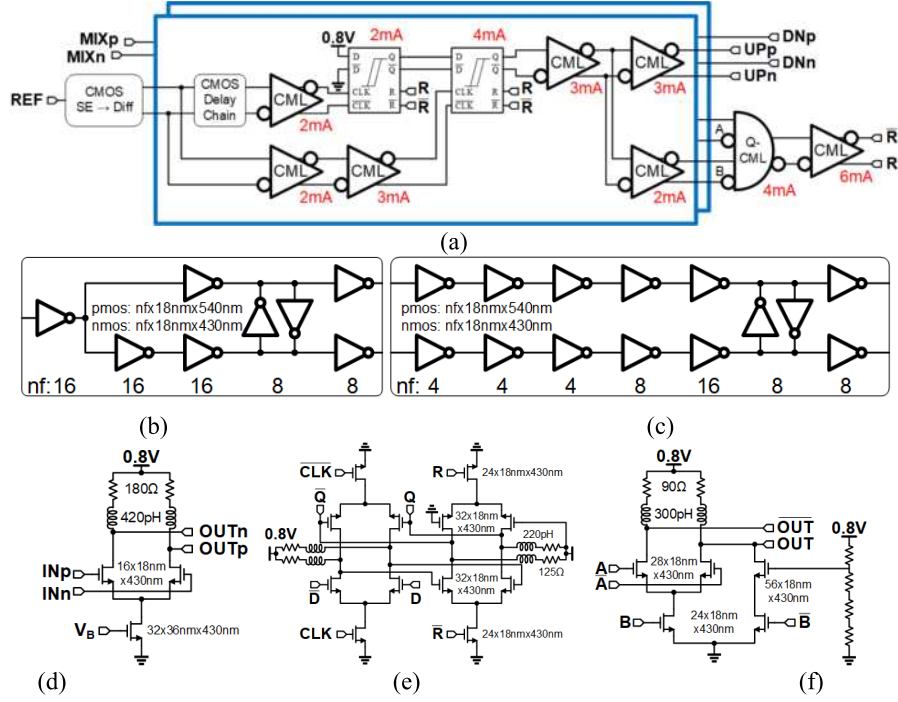


Fig. 10. (a) PFD block diagram showing (b) CMOS single-ended-to-differential converter, (c) CMOS delay chain, (d) 2 mA-sized CML buffer, (e) 4 mA-sized CML resettable latch, and (f) CML AND gate schematics used in the PFD.

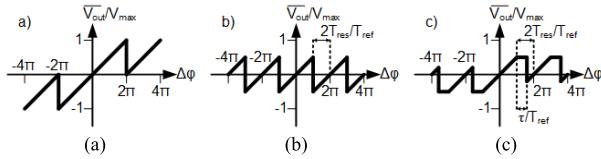


Fig. 11. Pictorial PFD characteristics for (a) ideal case, (b) nonideal with blind zone, and (c) improved PFD with reduced blind zone.

comparable to those of the varactors and negative resistance generator. The measured PN (symbols), compared in Fig. 9(b) to simulations (lines) at 2, 5 and 10 MHz offset, is better than  $-95$ ,  $-104$ , and  $-110$  dBc/Hz, respectively, over the entire tuning range.

The VCO buffer features a large-swing ( $>2 V_{pp}$  per side), series-stacked triple n-MOSFET cascode with double-sided gate contact and 18 nm physical gate length for improved isolation, to ensure robust operation of the static divider, and to maximize the voltage swing at the input of the 160 GHz doubler. The measured output power of the VCO-buffer breakout is between 9 and 11 dBm throughout the tuning range.

### C. 11 GHz Phase-Frequency Detector

In order to maximize the frequency of operation, the PFD features a combination of CMOS logic and (quasi-)CML blocks, as depicted in Fig. 10. Using a high reference frequency results in a challenging PFD design, since the reference signal period,  $T_{ref}$ , of 90–110 ps, is only 4–5 times larger than the reset pulsewidth,  $T_{res} = 23$ –26 ps. As shown in Fig. 11(a), this leads to the shrinking of the linear region

of the PFD from  $\pm 2\pi$  to

$$\varphi = \pm 2\pi \left( 1 - \frac{2T_{res}}{T_{ref}} \right). \quad (9)$$

The term  $(2T_{res}/T_{ref})$  is typically neglected in the PFD characteristic function when it is less than 0.01. The affected region is known as the blind (or dead) zone and can cause frequency slipping. To reduce the blind zone, the delay from the  $Q$  output of the resettable latch to its reset input should be minimized. Therefore, the smaller delay of quasi-CML blocks is preferred in the delay loop to realize the asynchronous resettable latch, and gate and inverters. To accommodate pulses as short as 23 ps at the output of the PFD, high-speed design techniques such as inductive peaking and biasing the quasi-CML gate transistors at half peak- $f_T$  current density are employed.

To alleviate the blind zone issue, the reference signals going to the latches in the flip-flop are proportionally delayed with respect to the delay in the feedback loop, as in [17]. To minimize the blind zone, simulations were conducted to adjust the delay by changing the backgate voltages of the p- and n-MOSFETs in the CMOS inverters that form the delay chain shown in Fig. 10(c). The optimal backgate bias voltages were found to be  $-2$  and  $+2$  V, respectively, and were fixed through resistive dividers in the fabricated chip. Assuming the total delay is  $\tau$ , as shown in Fig. 11(c), the new linear portion of the PFD transfer function is given by

$$\varphi = \pm 2\pi \left( 1 - \frac{2T_{res} - \tau}{T_{ref}} \right). \quad (10)$$

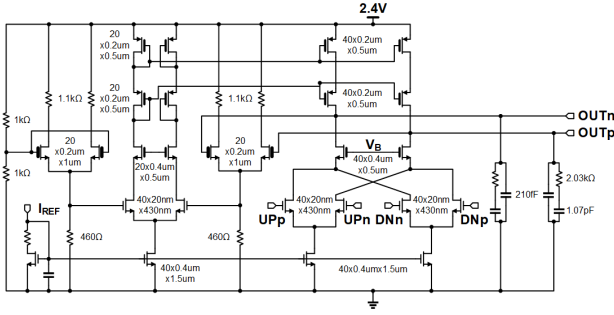


Fig. 12. Schematic of the charge pump and loop filter.

Therefore, careful selection of the delay can cancel the blind zone completely. However, a margin must be allowed as the condition  $\tau \leq 2T_{\text{res}}$  must be satisfied over process corners, otherwise, the PFD stops working. The simulated instantaneous PFD reset pulsewidth variation in time during a full bandwidth TX output ramp after layout parasitics extraction is presented in Section IV-C, in Fig. 21, as part of the simulations of the entire TX.

#### D. Charge Pump and Loop Filter

The charge pump schematic, depicted in Fig. 12, is a CMOS version of the SiGe BiCMOS telescopic cascode topology with common-mode feedback proposed in [14]. It employs thin oxide 0.8 V devices with 20 nm gate length in the n-MOSFET differential pairs for maximum speed, 200 nm gate length thick oxide 1.2 V common-gate and active load MOSFETs for high gain, and 1.8 V MOSFETs in the common-mode feedback. It operates from 2.4 V by taking advantage of the isolation properties of the buried oxide. The second-order loop filter is fully differential, with fixed resistor and capacitor values:  $R = 2.032 \text{ k}\Omega$ ,  $C_1 = 1.07 \text{ pF}$ , and  $C_2 = 212 \text{ fF}$ . The loop bandwidth is adjustable from 50 to 300 MHz by changing the charge pump current between 0.185 and 1.55 mA through a current reference,  $I_{\text{REF}}$ , provided from off-chip.

#### E. Static Divider Chain and SSB Mixer

The 80 GHz divider chain, Fig. 13(a), consists of 10 mA, quasi-CML static divide-by-2, 11 mA 40 GHz CML-to-CMOS converter, and 5 mA static divide-by-4 CMOS stages with a total power consumption of 20.8 mW from 0.8 V supply. To ensure robust operation from 0.8 V, the quasi-CML latch and CML-to-CMOS converter, depicted in Fig. 13(b) and (c), employ higher  $V_t$  (SLVT) n-MOSFETs with 20 nm gate length at the bottom and super low- $V_t$  (SLVT) n-MOSFETs at the top. Different  $V_t$  values are obtained simply by using different back-gate voltage of  $-0.5$  and  $2.5$  V, respectively.

The PLL IQ upconvert SSB mixer, Fig. 13(d), features a passive CMOS switch topology to maximize its linearity and is followed by a hard, rail-to-rail, limiter formed with a chain of CMOS inverters to suppress the image, and LO leakage spurs. The quadrature 0.8 V<sub>pp</sub> LO signals are provided by the static divider. Linear single-ended-to-differential conversion amplifiers are placed at the IF mixer inputs to boost the off-chip PLL  $I-Q$  modulation signals.

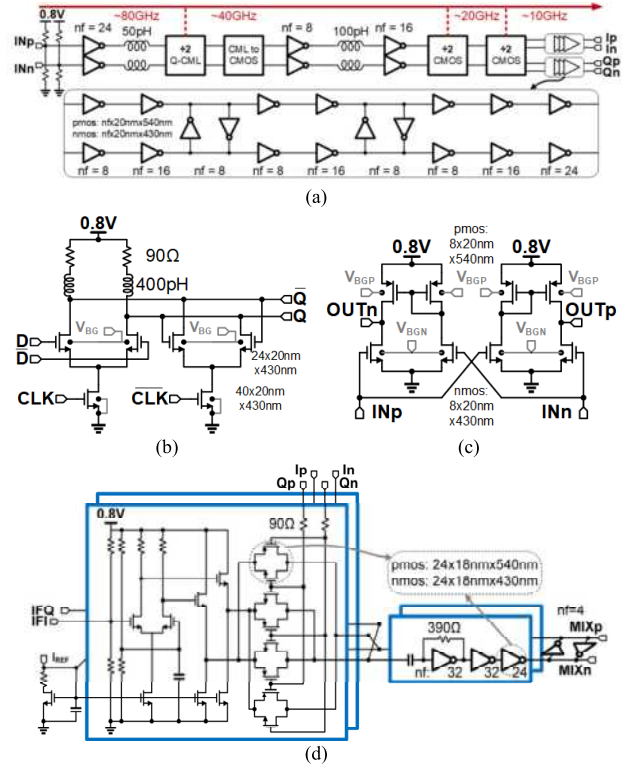


Fig. 13. Schematic for (a) 80 GHz static divide-by-8 chain, (b) quasi-CML latch, (c) CML-to-CMOS converter, and (d) 10 GHz SSB IQ mixer and input amplifier.

As mentioned, the PLL bandwidth was designed to minimize the integrated jitter up to 100 MHz based on a commercial 10 GHz DRO [13]. However, measurements of the PLL breakout and transceiver were conducted with a commercial synthesizer reference whose PN at 10 GHz is  $-116$ ,  $-139$ , and  $-144$  dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offset, respectively and a noise floor of  $-144$  dBc/Hz. As shown in Fig. 14, the measured PN of the 80 GHz PLL breakout is  $-91$ ,  $-98$ ,  $-112$ , and  $-117$  dB/Hz at 10 kHz, 100 kHz, 1 MHz, and 10 MHz offset, respectively, from 76 to 80 GHz. The values at 10 and 100 MHz offsets are limited by the spectrum analyzer noise floor of about  $-120$  dBc/Hz at 80 GHz. The measured PN in Fig. 14 is within 1 dB of the simulated value at 100 kHz and 1 MHz offset shown in Fig. 15. For offsets between 1 and 300 kHz, the simulated PN matches closely the scaled measured PN of the reference oscillator. Between 300 kHz and the loop bandwidth of 300 MHz, the simulated PN is 2–5 dB larger than the scaled reference PN due to noise contributions from the PFD, charge pump, and loop filter. At 40%, the reference PN is the main contributor up to 300 MHz. Measurements confirmed stability across all loop bandwidth settings. At the largest bandwidth setting of 300 MHz, the simulated PN shows  $<1$  dB of peaking.

## IV. IQ TRANSCIEVER DESIGN

### A. Frequency Doubler and LO Tree

The 160 GHz LO tree consumes 275 mW and consists of: 1) a frequency doubler with series stacked double cascode



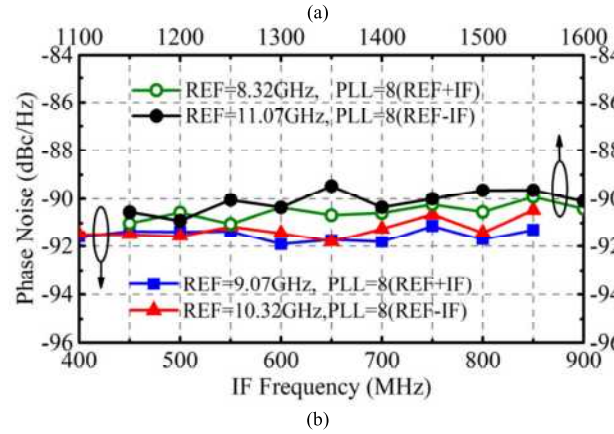
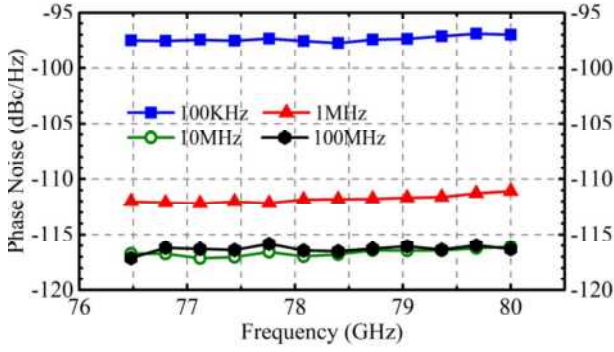


Fig. 14. Measured PN of the 80 GHz PLL breakout (a) as a function of output frequency and offset frequency and (b) at 10 kHz offset as a function of the IF input and reference frequencies.

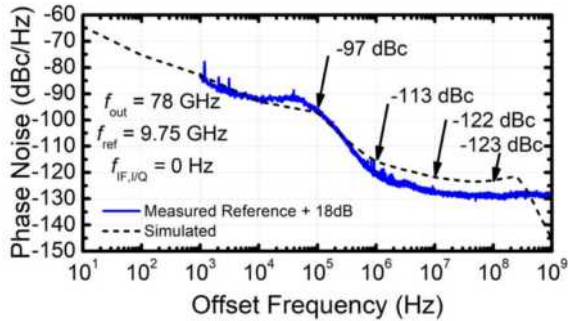


Fig. 15. Simulated PLL PN at 78 GHz. The measured PN of the 9.75 GHz reference is also shown with ideal  $\times 8$  multiplication.

biased from 2.4 V, as shown in Fig. 16(a); 2) identical cascaded large-swing cascode stages with  $40 \Omega$  input and output impedance and biased from 1.6 V supply, Fig. 16(b); 3)  $40 \Omega$  transmission lines; and 4) lumped  $40 \Omega$  Wilkinson power splitters whose schematic is shown in Fig. 17(a). All MOSFETs have minimum gate length of 18 nm and two-sided gate contact 720 nm finger width with  $2\times$  metal pitch to maximize power gain and to satisfy electromigration rules at  $110^\circ\text{C}$  and large drain current densities up to  $0.4 \text{ mA}/\mu\text{m}$ . The bottom differential pair in the doubler uses high- $V_t$  (HVT)

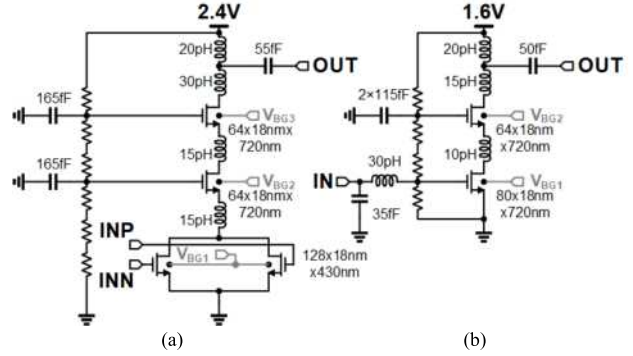


Fig. 16. Schematic of the 160 GHz (a) doubler and (b) LO amplifier stages.

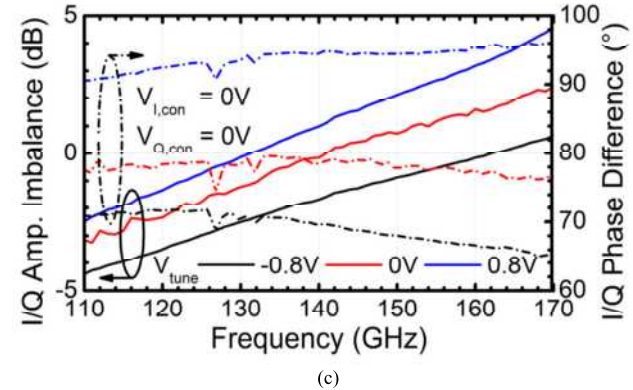
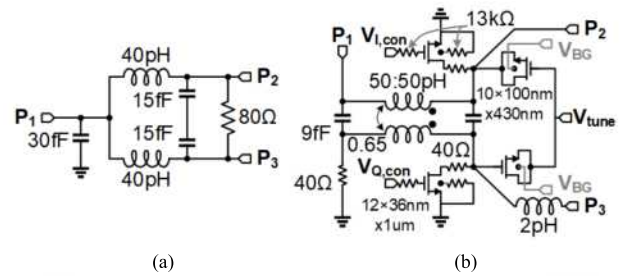


Fig. 17. Lumped D-band (a) Wilkinson power splitter and (b)  $90^\circ$  hybrid schematics. (c) Measured amplitude imbalance control and phase difference control of the  $90^\circ$  hybrid breakout.

*n*-MOSFETs biased in class B. All the other transistors are SLVT devices operating in class AB mode. The measured insertion loss of the Wilkinson splitter breakout varies between 1.2 and 1.9 dB from 110 to 170 GHz.

### B. Lumped IQ Hybrid

In addition to the symmetry of the Gilbert-cell layout, the LO leakage and image rejection of the TX upconvert and RX downconvert mixers depends on the amplitude and phase errors of the IQ hybrid and on the common-mode rejection of the transformers used for single-ended-to-differential conversion. The same D-band transformer-based  $90^\circ$  hybrid, whose schematic is shown in Fig. 17(b), is included in TXs and RXs as IQ power combiner and power splitter, respectively. It is designed for a characteristic impedance of  $40 \Omega$  and

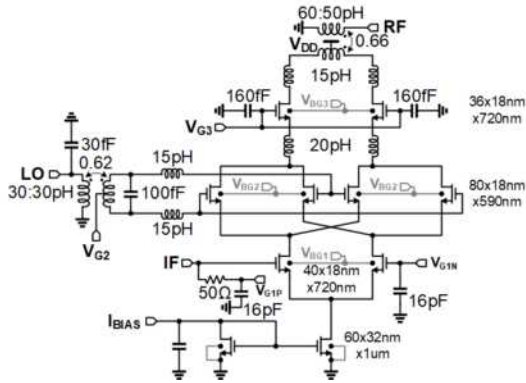


Fig. 18. D-band TX up-convert mixer schematic.

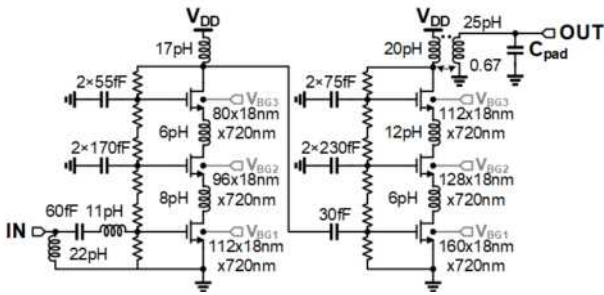


Fig. 19. D-band PA schematic.

features independent phase control through  $V_{\text{tune}}$ , using AMOS varactors, and IQ amplitude imbalance control (via  $V_{\text{Qcon}}$  and  $V_{\text{Icon}}$ ) using shunt variable-resistance n-MOSFETs in series with  $40 \Omega$  polysilicon resistors. As shown in Fig. 17(c), the independent IQ amplitude and phase difference control range were verified in measurements on a breakout of the  $90^\circ$  hybrid. They are  $\pm 1$  dB and  $80^\circ$ – $90^\circ$ , respectively, from 140 to 160 GHz.

### C. Transmitter

Each TX consists of an IQ linear upconverter and a PA with a total nominal power consumption of 192 mW from 2.4 V supply. The schematic of one of the two double-balanced Gilbert-cell mixers that, along with the  $90^\circ$  hybrid form the IQ upconverter, is depicted in Fig. 18. It has single-ended IF input to reduce the number of signal pads and die size. Single-ended-to-differential conversion is performed in the input differential transconductor. The mixer employs a large swing common-gate n-MOSFET differential pair at its output to increase the gain and output voltage swing, as well as a transformer for differential-to-single-ended conversion. The latter is needed to drive the single-ended IQ hybrid. Each IQ upconverter consumes a total of 30 mA from a supply of 2.4 V.

The 10 dB gain PA, shown in Fig. 19, has two stages featuring series stacked triple cascodes with gradual 20% transistor size reduction in the upper stack to maximize bandwidth and gain [18] at D-band. The output stage is identical to the one in [19] except for the transformer output matching network

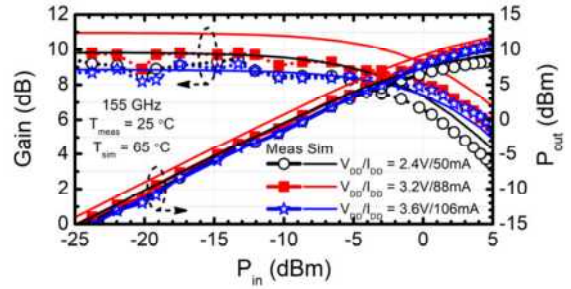


Fig. 20. Measured (symbols) and simulated (lines) D-band PA gain and output power versus input power at 155 GHz. Measured on standalone PA breakout.

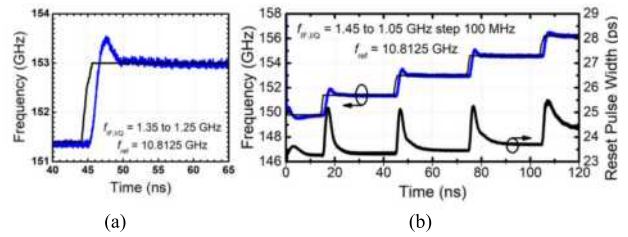


Fig. 21. Simulated (blue) (a) settling time and (b) stepped-frequency ramp with  $T_{\text{step}} = 30$  ns at the TX output also showing the corresponding PFD reset pulsewidth variation in time (black thick lines). For comparison, the frequency scaled IF PLL input signal is shown with black thin lines.

which also provides dc blocking and ESD protection. Output power and gain control are implemented by changing the  $V_{\text{DD}}$  of the two stages between 1.8 and 3.6 V. It draws 50 mA from the nominal 2.4 V supply (120 mW) and has a saturated output power of 9 dBm,  $P_{01 \text{ dB}}$  of 5 dBm, and 3% PAE, as shown in Fig. 20. The saturated output power of the PA increases to 11 dBm when the power supply voltage is raised to 3.6 V, corresponding to 1.2 V per transistor. The latter is still a safe operating voltage for the thin oxide MOSFETs in this technology [20]. Finally, to illustrate the full functionality of the TX, Fig. 21 reproduces the simulated settling time, smaller than 20 ns, and the transient waveforms after RC layout parasitics extraction of a stepped-frequency carrier signal at the output of the TX covering the 150–156 GHz range with four short 30 ns wide, 1.5 GHz tall steps.

### D. Receiver

Each RX consists of an LNA, the  $90^\circ$  hybrid from Fig. 17(b), and two double-balanced Gilbert cell mixers. The LNA, Fig. 22, consumes 20 mA from 1.6 V supply and features three cascode stages with 18 nm gate length and 720 nm gate finger width SLVT n-MOSFETs contacted on both sides of the gate and biased at the minimum noise figure current density of  $0.25 \text{ mA}/\mu\text{m}$ . A transformer is placed at the input for ESD protection and to prevent dc coupling to the antenna. The LNA breakout has a measured peak gain of 19.8 dB centered at 149 GHz with the 3 dB bandwidth extending from 144 to 155 GHz, a saturated output power of 5 dBm and an input compression point of  $-20$  dBm. As shown

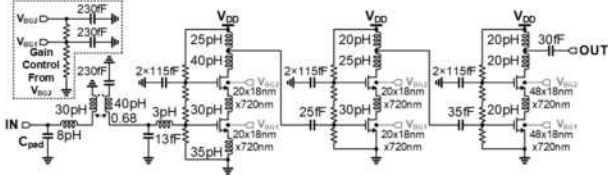


Fig. 22. LNA schematic.

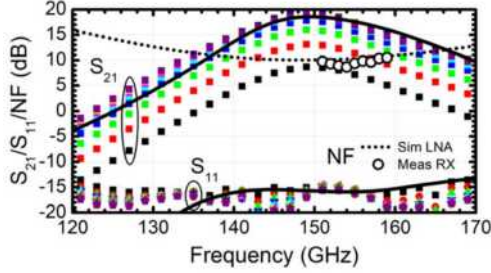


Fig. 23. Comparison between the measured (symbols) LNA breakout  $S_21$  at  $V_{DD} = 1.6$  V as a function of the backgate voltage from 4 to  $-0.5$  V. Simulated (solid lines)  $S_{21}$  at peak gain setting shows reasonable agreement. Simulated LNA NF (dotted lines) compared to measured SSB NF of full RX.

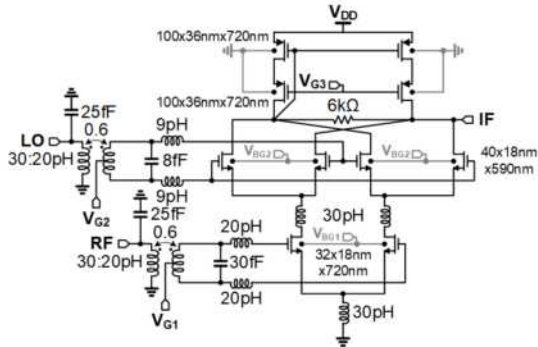


Fig. 24. D-Band RX down-convert mixer schematic.

in Fig. 23, variable gain control of 12 dB, between 8–20 dB gain, is achieved by changing the backgate voltages of the transistors in all cascode stages in tandem between  $-0.5$  and 4 V (corresponding to  $I_{DS}/W = 0.1\text{--}0.4$  mA/ $\mu\text{m}$ ), without loading the mm-wave signal path.  $S_{11}$  remains  $< -14$  dB from 120 to 170 GHz, irrespective of the gain setting. As can be seen from Fig. 23, there is reasonable agreement between measurements and simulations. The simulated LNA NF (black dotted lines), in the 9.5–10 dB range, is about 0.5–1 dB larger than the measured SSB NF of the RX (open black circles).

The DB downconvert mixer schematic is depicted in Fig. 24. It uses a Gilbert cell topology with an active cascode current mirror load to maximize the conversion gain. The 32 nm  $\times$  18 nm  $\times$  720 nm n-MOSFETs in the transconductor are biased at 0.3 mA/ $\mu\text{m}$  as a trade-off between low noise figure and linearity and draws 15.5 mA from the 1.6 V supply. Thus, the IQ mixer consumes 25 mW with an RX total of 87.5 mW.

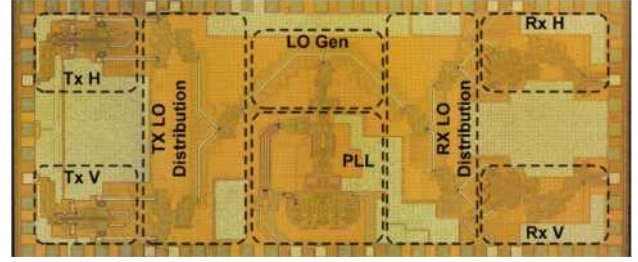


Fig. 25. Chip microphotograph: 1.1 mm  $\times$  2.5 mm.

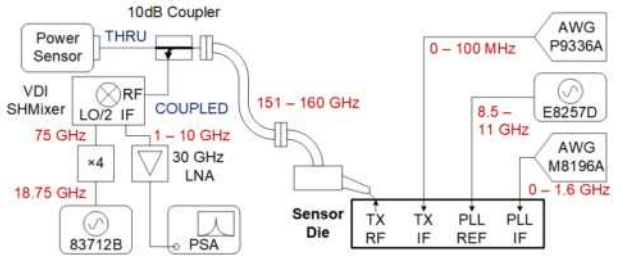


Fig. 26. Setup for TX output power and output spectrum measurements.

## V. SENSOR TRANSCIEVER FABRICATION AND CHARACTERIZATION

The sensor circuit and associated breakouts were manufactured in GlobalFoundries' 22 FDX technology [21] which features 0.8 V FDSOI MOSFETs with a minimum gate length of 18 nm, 1.2 V, and 1.8 V MOSFETs and varactors, and thick metal and thick dielectric back-end-of-line option with two 3  $\mu\text{m}$ -thick copper layers. The mm-wave performance of fully wired n- and p-MOSFETs, varactors, cross-coupled VCOs, and of series stacked large-swing cascodes was characterized over temperature and reported in [16] and [19], respectively. A maximum available power gain of over 8 dB was measured up to 170 GHz in the triple stacked cascode used as the output stage of the sensor PA. Fig. 25 reproduces the 2.5 mm  $\times$  1.1 mm sensor die microphotograph.

The sensor transceiver performance was measured on die, using waveguide probes at the D-band inputs and outputs of the two RXs and two TXs. The test setup for TX measurements is sketched in Fig. 26. A D-Band 10 dB coupler with an ELVA D-band power sensor connected at its THRU output were used to measure the output power of the unmodulated carrier directly, while a D-band VDI downconverter followed by a power spectrum analyzer (PSA) was connected at the coupled output to monitor frequency and the output spectrum and to measure the image rejection and the LO leakage of the transmit upconverter. The wafer probe, coupler, and VDI downconverter losses were calibrated out based on S-parameter measurements with an offset-short calibration. Over 15 different dies were probed. Less than 1 GHz tuning range and 1 dB output power variation were observed from die to die. Fig. 27 shows the measured output power and image rejection at the horizontal (TXH) and vertical polarization (TXV) TX pads for a 10 MHz single-ended, 40 mV amplitude signal applied at the IF inputs of each TX. Excellent matching

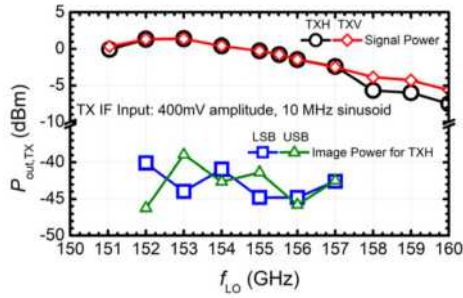


Fig. 27. Measured output signal and image power versus LO frequency for the vertical- and horizontal-polarization TXs in the sensor transceiver.

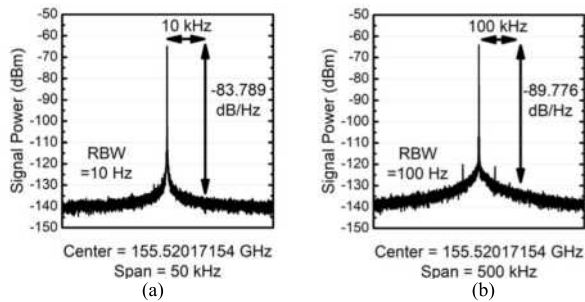


Fig. 28. Measured PN at 155 GHz at the TX output at (a) 10 and (b) 100 kHz offset using the setup in Fig. 29.

between the two TXs in the sensor die can be observed across the entire 151–160 GHz PLL locking range, with the peak output power per TX of 2 dBm, backed off from the 1 dB compression point, and centered on 152.5 GHz.

Accurate PN measurements at D-band are tricky due to setup losses and high noise floor. For comparison, several test setups, each with its own advantages and drawbacks were employed. To facilitate comparison with the measured PN of the standalone 80 GHz PLL breakout, in all the TX PN measurements the carrier was not modulated and the IF-PLL inputs were ac grounded. The measured PN of  $-83.7$  and  $-89.7$  dBc/Hz at 10 and 100 kHz offset, respectively, from the 155 GHz carrier is reproduced in Fig. 28. It was obtained with the setup in Fig. 29 which provides the best accuracy at offset frequencies below 100 kHz. As can be observed from Fig. 28, PN measurements directly at the D-band TX output using the built-in LO of the Keysight E4448A PSA and the Farran D-band harmonic mixer are limited by the noise floor of the test setup for offset frequencies larger than 100 kHz. To prove it, Fig. 30 shows the PN (blue curve) as a function of offset frequency measured up to 1 GHz using the setup in Fig. 26 with the VDI downconverter which has lower conversion loss, but which requires an external LO. Its IF output was applied to a Keysight UXR1002A 110 GHz bandwidth RTOS used as a PN analyzer, replacing the PSA in Fig. 26. In this case, the noise floor is significantly improved above 100 kHz but the PN contribution of the external LO source is also included and dominates at offset

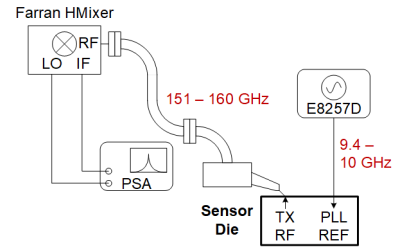


Fig. 29. Setup used for TX output PN measurements at close-in offset frequencies  $<100$  kHz.

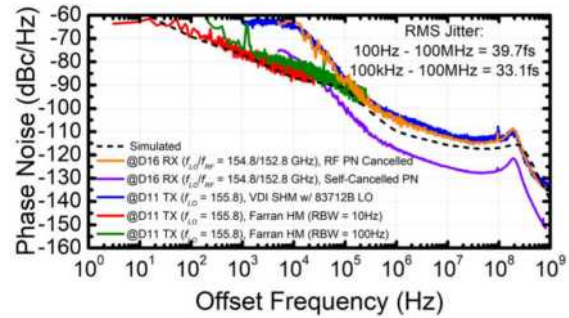


Fig. 30. Comparison of the measured (lines) and simulated (dashed) PN on dies D11 and D16 at the TX and RX outputs as a function of offset frequency using different downconvert mixers and mm-wave signal sources.

frequencies below 1 MHz, resulting in measured PN values of  $-87.5$ ,  $-107.17$ , and  $-114.8$  dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offset, respectively.

To better capture the limitations of each PN test setup and measurement approach, Fig. 30 also shows the comparison of the PN at 155 GHz measured at the TX output (red, green, and blue) and RX output (orange and purple) with (green, red) and without (blue) canceling the PN of the external LO signal. For the RX PN measurements, the setup in Fig. 31 was used. These plots indicate that up to 100 kHz offset, PN should be measured at the TX output with the PSA using the setup in Fig. 28 with 10 Hz resolution bandwidth and the harmonic Farran mixer driven by the PSA LO (red and green curves). For higher offsets, the RX PN setup in Fig. 31 should be used with the PN of the external D-band input signal source canceled (orange curve). The best estimate of the actual TX PN is thus obtained by choosing the minimum value between all measured PN curves at a particular offset frequency.

Fig. 30 also includes a purple trace, measured using the RX PN setup in Fig. 31, where the  $Q$ -output of the sensor RX is used as external clock signal for the RTOS to measure the PN at the  $I$ -output of the sensor RX. This arrangement cancels the PN of both the internal PLL and of the external 155 GHz input signal source. It further reduces the measured PN by at least 10 dB at all offset frequencies from 10 kHz to 1 GHz. The PN captured by this trace, lower than  $-120$  dBc/Hz above 1 MHz, is due only to the combined contributions of the sensor  $I$  and  $Q$  RX paths (LNA, mixer, IF amplifier, and LO-tree branches)

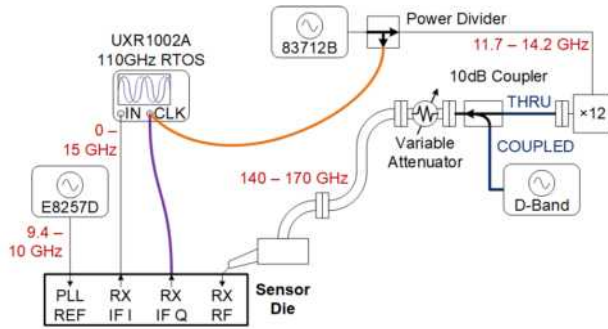


Fig. 31. Setup used for RX two-tone linearity and PN measurements at offset frequencies > 100 kHz. The COUPLED D-band signal source was only used for linearity measurements. For PN measurements using the UXR1002A, the RF signal PN is canceled by using the HP83712B as the reference for the RX IF output (orange) and the PN of the RX IF is self-canceled using the Q output as a reference for the I output (purple).

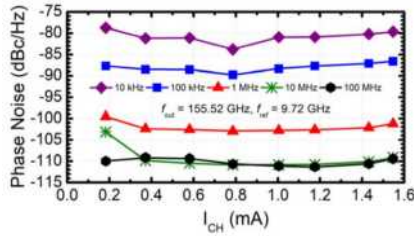


Fig. 32. Measured PN at the TX D-band output as a function of charge pump current and offset frequency.

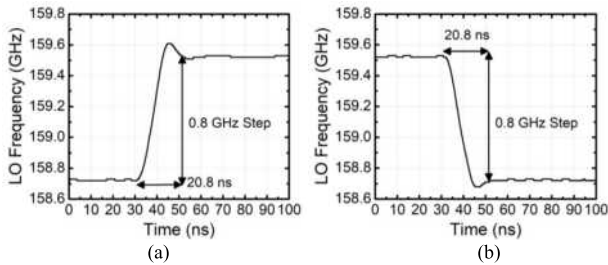


Fig. 33. Measured PLL 1% settling time at the output of the TX for (a) rising and (b) falling frequency step.

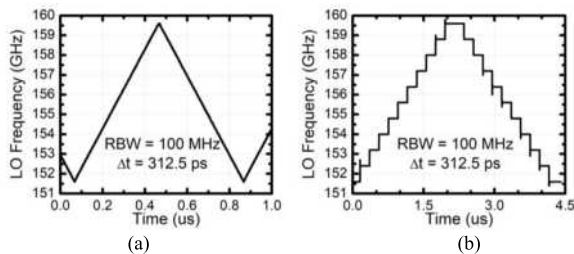


Fig. 34. Measured (a) 800 ns V-shaped full FMCW chirp at the output of the TX and (b) stepped frequency chirp at the output of the TX.

and whose noise is uncorrelated, and of the RTOS. It confirms that the  $1/f$  noise corner of the downconvert mixers is smaller

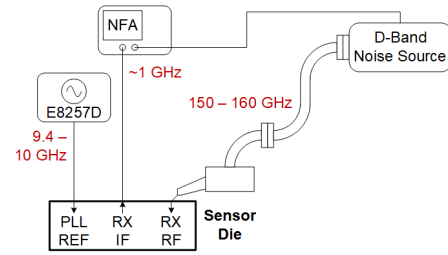


Fig. 35. Setup used for RX noise figure measurements.

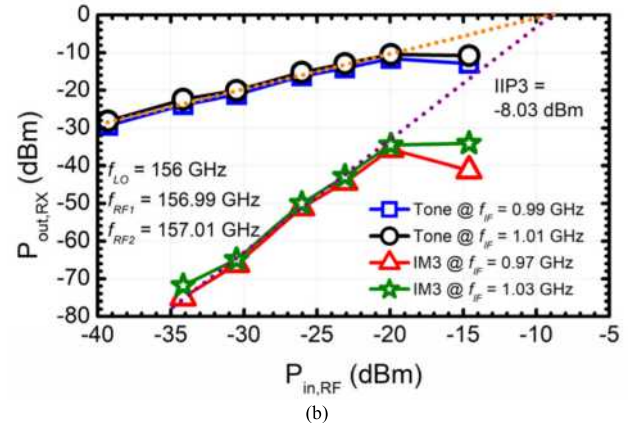
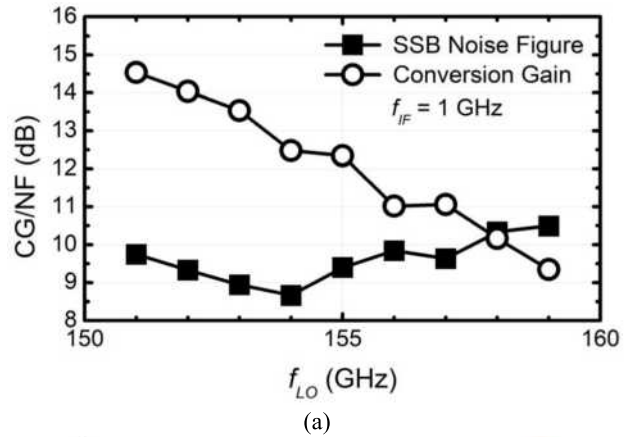


Fig. 36. Measured RX (a) conversion gain and noise figure versus LO frequency and (b) RX IIP3 at 156 GHz.

than 1 MHz. The simulated TX PN (black dashed lines) is also plotted in Fig. 30, showing excellent agreement with measurements for frequency offsets smaller than 300 kHz, where the PN of the reference dominates, as in Fig. 15. Between 300 kHz and 200 MHz, simulations underestimate the PN by 2–3 dB. This could be explained by a higher noise floor of the reference oscillator in the measurement setup than assumed in simulation or by lower TX output power in measurements than in simulation.

Fig. 32 summarizes the PN measurements at the 155.5-GHz TX output as a function of frequency offset and charge pump current. In all cases, the best performance is obtained for  $I_{CH} = 0.79$  mA and is 6–7 dB higher than that measured at the 80 GHz output of the PLL breakout in Fig. 14.

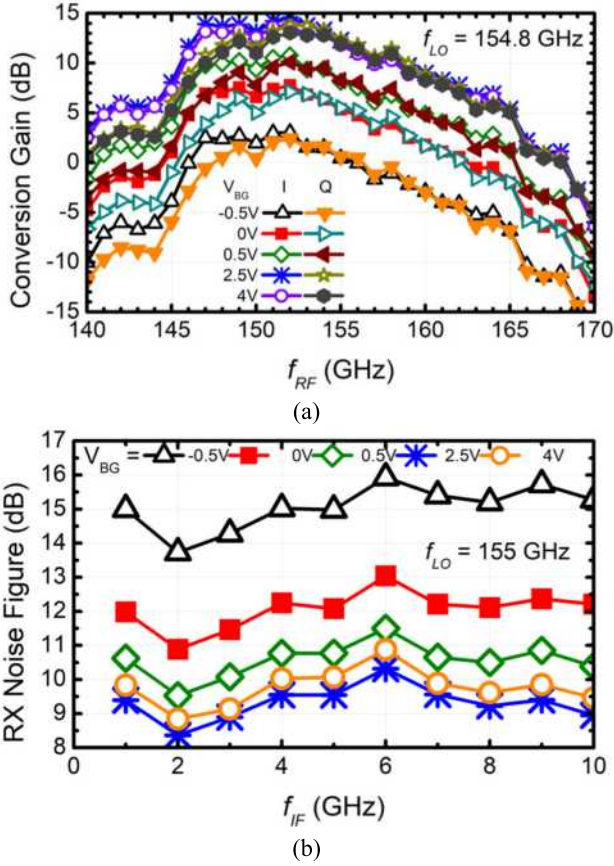


Fig. 37. Measured (a) RX downconversion gain control and IQ matching versus RF frequency and (b) SSB noise figure versus IF frequency for the same backgate voltages used to control the gain.

Figs. 33 and 34 demonstrate the short settling time, less than 30 ns, of the TX output, limited by the speed of the AWG used to drive the IF input of the PLL, as well as 800 ns V-shaped FMCW, Fig. 34(a), and stepped-frequency, Fig. 34(b), chirps spanning the full 151.5–160 GHz bandwidth of the radar sensor transceiver in ten 160 ns wide and 850 MHz tall steps.

The RX noise figure was measured using an Elva D-Band noise source at the RX input and an Agilent 0.1–26.5 GHz NF analyzer (NFA) connected at the RX IF output, as depicted in Fig. 35. The linearity of the RX was characterized by applying single-tone and two-tone inputs at the D-band RX input and measuring the spectrum at the RX baseband output for different LO frequencies, using the setup in Fig. 31. The RX performance is summarized in Figs. 36 and 37 with a peak conversion gain of 15 dB per  $I$  and  $Q$  output at 151 GHz, an IIP3 of  $-8$  dBm, and an RX SSB NF between 7.5 and 10 dB throughout the 146–156 GHz RF bandwidth of the RX. Over 12 dB of gain control is demonstrated by changing the backgate voltages (i.e., the drain current density) of the LNA cascodes in Fig. 37(a). The measured mismatch between the conversion gains of the  $I$  and  $Q$  outputs of the RX is  $<1$  dB in the 145–170 GHz range.

TABLE II  
PARAMETERS FOR MEASURED OFDM MODULATED RAMP (FIG. 38)

Description	Parameter	Value
Fundamental frequency	$f_0$	155.52 GHz
RF modulation bandwidth	$B_{MOD}$	8 GHz
Number of frequency steps	$S_b$	40
IF bandwidth	$B_{IF}$	100 MHz
Number of OFDM symbols	$M_s$	2
OFDM subcarrier spacing	$\Delta f_c$	8 MHz
LO frequency step	$T_{step}$	200 ns
PLL settling time	$T_{settling}$	$< 30$ ns
Ramp duration	$T_{mod}$	4 $\mu$ s
Linear ramp slope	$k_r$	0.08– 8 GHz/ $\mu$ s
PLL reference	$f_{REF}$	8.52 GHz
PLL IF input frequency range	PLL-IQ $BW$	0.95–1.45 GHz

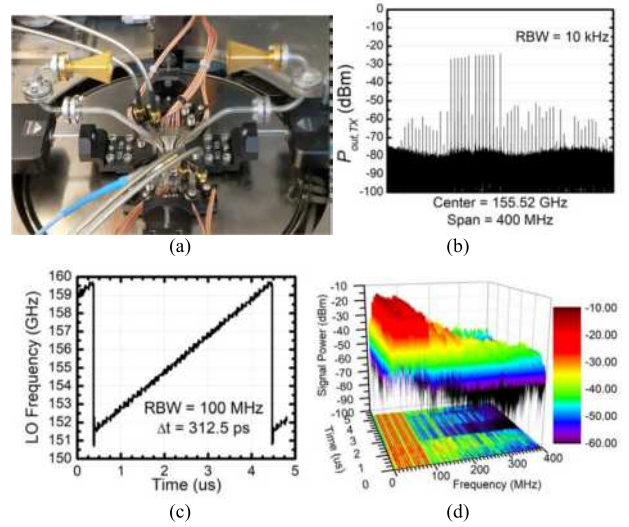


Fig. 38. Through-the-air loopback measurements with stepped, OFDM modulated ramp. (a) Setup, (b) TX output spectrum at fixed carrier frequency, (c) TX output stepped-frequency trace with 40 and 100 ns wide steps and 100 MHz OFDM modulation (Table II), and (d) power versus frequency and time at the RX IF output.

Finally, a through-the-air transmit-receive sensor transceiver loopback link was established by mounting antennas face-to-face at the output of one TX and the input of one RX, as illustrated in Fig. 38(a). Full-bandwidth frequency chirps with 40- and 100 ns wide steps, Table II, were generated with an AWG at the PLL IF input which were modulated with 100 MHz OFDM signals from a second AWG applied at the TX IF input. The OFDM spectrum and spectrogram trace measured at the TX output are illustrated in Fig. 38(b) and (c), respectively, along with the measured power versus time and frequency spectrum at the RX IF output in Fig. 38(d). As expected, the RX IF spectrum occupies only 100 MHz of bandwidth, despite the fact that the TX output signal bandwidth is 8 GHz. A link to a loopback video is available at [22].

TABLE III  
COMPARISON OF STATE-OF-THE-ART D-BAND TRANSCEIVER PERFORMANCE

Ref.	Tech. $f_i/f_{MAX}$	Arch.	Freq. (GHz)	Tx Pout (dBm)	PN @ (dBc/Hz)		RMS Jitter	Settling Time/ PLL Loop Bandwidth	Ref. Freq.	Rx Gain (dB)	Rx NF (dB)	Input $P_{1dB}$ (dBm)	$P_{DC}$ (mW)
					100kHz	1MHz							
[23]	28-nm CMOS	Tx, Rx	127-154	11.5 <sup>†</sup>	-	-	-	-	-	80	8	-	500 <sup>†</sup>
[24]	22-nm FDSOI	Tx, Rx	123-146	2.8	-	-	-	-	-	27	8.5 <sup>***</sup>	-30	394 <sup>†</sup>
[25]	SiGe BiCMOS 300/500GHz	Tx, Rx	115-155	13	-	-	-	-	-	65	7.5-10	-9	2350 <sup>†</sup>
			135-170	13	-	-	-	-	-	65	8-11	-8	3400 <sup>†</sup>
[26]	SiGe:C HBT 170/250GHz	Tx, Rx	155-165	1	-	-	-	-	-	-	17 <sup>**</sup> DSB	-4 <sup>**</sup>	749
[27]	SiGe BiCMOS 220/280GHz	Tx, 2Rx, PLL	145-168	-4	-68	-82	-	-	600 MHz	27	12	-	1800 <sup>†</sup>
[10]	SiGe BiCMOS 170/250GHz	2-chip: Tx, Rx, PLL	120-170	3	-80	-87@122 GHz	288.7 nm	1-2 MHz	100 MHz	8.3	19.3	-2.9	3750/338 <sup>***</sup>
[5]	SiGe BiCMOS	4x,Tx,Rx, int-PLL	149-165	-1	-80	-87	-	-	916 MHz	-2	25	-	-
[28]	SiGe BiCMOS 300/500GHz	Monostatic Tx, Rx	147-166	3	-69	-78	-	700 kHz	2.3-2.6 GHz	19	15.5	-10	5400
		Bistatic Tx, Rx	147-166	13	-69	-78	-	700 kHz	2.3-2.6 GHz	24	11	-18	8400
[29]	SiGe BiCMOS 300/500GHz	2Tx, 2Rx, PLL	77-81	9	-80	-80	-	1 MHz	100 MHz	24	7.2 <sup>**</sup>	-10	3254
			154-162	13	-74	-74	-	1 MHz	100 MHz	24	-	-	-
<b>This work</b>	<b>22-nm FDSOI</b>	<b>2Tx, 2Rx, PLL</b>	<b>151-160</b>	<b>2 per Tx</b>	<b>-90</b>	<b>-107</b>	<b>39.7/33.1 fs</b> <b>100Hz/100kHz-100MHz</b>	<b>&lt; 30ns</b>	<b>8.4-11.1 GHz</b>	<b>15<sup>++</sup></b>	<b>7.5-10</b>	<b>-20</b>	<b>1130<sup>†</sup></b>

\*EIRP \*\*simulated. \*\*\*synthesizer only. †chirp synthesizer not included. ++measured in 50-Ω load. Simulated 4.5 dB higher with intended 300-Ω load.

TABLE IV  
COMPARISON OF STATE-OF-THE-ART 80 GHz PLLS

Ref.	Tech. $f_i/f_{MAX}$	Arch.	Freq. (GHz)	Pout (dBm)	PN @ (dBc/Hz)			Jitter rms	Settling Time/ PLL Loop Bandwidth	Ref. Freq.	$P_{DC}$ (mW)
					10kHz	100kHz	1MHz				
[8]	SiGe BiCMOS 170/250 GHz	Offset, Frac-N	68-92	6	-97	-98	-94	70 fs 10kHz-10MHz	2 MHz	167 MHz	1555
[14]	SiGe BiCMOS 220/280GHz	Integer-N	80-100	-3	-84	-93	-100	166 fs 1MHz-1GHz	2 MHz	5 GHz	1150 <sup>†</sup>
[30]	SiGe BiCMOS 240/270GHz	Frac-N	80-100	6-8	-89	-90	-99	82.4 fs 10kHz-20MHz	30 MHz	1.6875 GHz	200/275 <sup>*</sup>
[31]	SiGe BiCMOS 80/90GHz	Integer-N	64-81	-2.4	-90	-92	-106	-	< 100 ns <sup>**</sup>	1.25 GHz	431 <sup>†</sup>
[32]	SiGe BiCMOS 220/280GHz	Integer-N	92.7-100	6	-85	-92.5	-102	71 fs 1MHz-1GHz	20 MHz	3 GHz	469.3 <sup>†</sup>
[12]	28-nm CMOS	SS-PLL	8.3-11.7	-	-87/ -69 <sup>++</sup>	-105/ -87 <sup>++</sup>	-109/ -91 <sup>++</sup>	314 fs/2.5 <sup>++</sup> ps 10kHz-81MHz	3 MHz	80 MHz	11.7
[33]	SiGe BiCMOS	Dual path Frac-N	75-83	6.5	-70	-72	-97	-	200 kHz	125 MHz	590
<b>This Work</b>	<b>22-nm FDSOI</b>	<b>SSB, Integer-N</b>	<b>76-80</b>	<b>9-11</b>	<b>-91</b>	<b>-97</b>	<b>-113</b>	<b>34/52 fs</b> <b>10kHz-20/100 MHz</b>	<b>30ns/200MHz</b>	<b>8.4-11.1 GHz</b>	<b>300<sup>†</sup></b>

\*PLL/TX Element. \*\*simulated. †chirp synthesizer not included. ++upconverted phase noise at 80 GHz assuming ideal 8x multiplier (+18 dB).

## VI. CONCLUSION

A novel 80 GHz fundamental frequency PLL architecture with record PN and settling time was demonstrated and integrated into a 22 nm FDSOI, first-ever 160 GHz stepped-frequency and FMCW carrier radar sensor transceiver with OFDM modulation. The record performance and new functionality are the result of the low loop division ratio of

only 8, enabled by an ultra-fast 11 GHz bandwidth PFD and charge pump, and by the linear SSB upconvert mixer placed in the PLL. The latter relaxes the PN specification of the low frequency DDS or DAC required to generate the linear FMCW and stepped-frequency carrier. Ultra-fast 800 ns FMCW and stepped-frequency chirps with OFDM modulation were demonstrated in a through-the-air loopback link.

The tuning range at the output the TX measured across 17 dies was 150.53–159.138 GHz with standard deviations of 1.14 and 1.179 GHz, respectively, indicative of the excellent performance repeatability of the 22 nm FDSOI CMOS technology at D-band.

Table III summarizes the sensor transceiver performance and compares it with that of state-of-the-art D-band transceivers, while the 80 GHz PLL breakout is compared with 80 GHz automotive radar and lower frequency PLLs in Table IV. The proposed transceiver demonstrates at least 7 and 10 dB better PN at 1 MHz offset than all previous work at 80 and 150 GHz, respectively, at least three times smaller PLL settling time and the highest level of integration for a D-band radar transceiver. The measured PN at 10 and 100 kHz offsets is limited by the reference signal source. At 1–100 MHz offsets, simulations show that the reference PN is still the dominant contributor, at about 40%, with the other 60% coming from the PFD, charge pump, and loop filter. Therefore, a further 10 and 2 dB PN improvement, respectively, is expected at all offset frequencies below 1 MHz, and in the 1–100 MHz range, respectively, with a commercial 10 GHz DRO reference.

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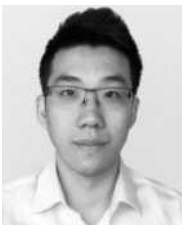
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