Design Considerations for Spin Readout Amplifiers in Monolithically Integrated Semiconductor Quantum Processors

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***Abstract*— The high frequency performance of all active and passive devices in a production 22nm FDSOI CMOS technology was measured up to 40 GHz over temperature down to 3.3 Kelvin, targeting applications in cryogenic and quantum computing ICs. It was found that the quality factor of the passives and the f_T and f_{MAX} of both p- and n-MOSFETs improved at 3.3 K. More importantly for circuit design, the peak-f_T and peak-f_{MAX} current densities, and the MOM capacitor and polysilicon resistor values show no variance with temperature. This information and the measured I-V characteristics of electron and hole single- and double-quantum dot structures, measured at 2 K and representative of qubits, were used to design monolithically integrated double quantum dots with readout transimpedance amplifiers output matched to 50 Ω. Transimpedance gain, S_{21}, and bandwidth of 108 dBΩ, 19 dB, and 7.5 GHz, respectively, were measured at 300 K with only 4.5 mW power consumption and S_{22} < -10 dB up to 60 GHz.**

***Keywords*—cryogenics, electron-spin, hole-spin, qubit, semiconductor quantum dot, silicon germanium, transimpedance amplifier**

I. Introduction

One of the biggest hurdles to realizing physical quantum computers has been the development of a reliable hardware platform capable of integrating billions of identical qubits monolithically. The current approach is for qubit array chips to be separately packaged and operated at a base temperature below 100 mK, with their microwave control and readout electronics located on a separate die at 1-4 K and accessed via a large number of 50Ω coaxial cables [1]. This multi-chip approach has historically been motivated by several factors, despite the interconnect and fidelity challenges which arise from it [2], [3]. More specifically, it has been a challenge to accommodate high yield, high f_T/f_{MAX}, transistors and microwave and analog-mixed-signal (AMS) circuits in the experimental laboratory technologies in which the silicon qubits are manufactured [4]. Additionally, state-of-the-art cryogenic cooling systems have also been limited in the dissipated power they can remove while maintaining a certain temperature: a few mW at 100 mK and ~2 W at 4 K [1]. More recently however, there has been mounting evidence that Si-based electron- and hole-spin qubits need not be limited to sub-1K temperatures [5] and that they are realizable in production CMOS technology, where they can be integrated with classical readout and control electronics [7]. In this paper, we describe for the first time the cryogenic high-frequency performance of all the active and passive components of a commercial 22nm FDSOI CMOS technology [6] and investigate the design considerations and design methodology for monolithically integrated quantum dots (QDs) with readout circuitry achieving record gain and bandwidth.

II. Cryogenic Technology Characterization

A full set of MOSFETs, 4µm x 7.5µm metal-oxide-metal (MOM) caps, 100Ω and 200Ω poly resistors, and the associated 6µm x 400µm de-embedding transmission line structures were designed and fabricated in two variants of the 22nm FDSOI CMOS process [6] with thin metal and thick metal BEOL, respectively. A microphotograph of the test chip is reproduced in Fig. 1. All 3.3K MOSFET measurements shown are with floating back gates due to limitations of the cryogenic setup.

Figs. 2-4 compile the measured transconductance, f_T, f_{MAX}, gate, R_G, and source, R_S, resistances for fully metallized, single-gate contact *n*- and *p*-channel MOSFETs with 40 gate fingers, 20nm gate length, 1x source/drain contact pitch, and gate finger widths of 430 nm and 590 nm, at 3.3 K and 300 K.

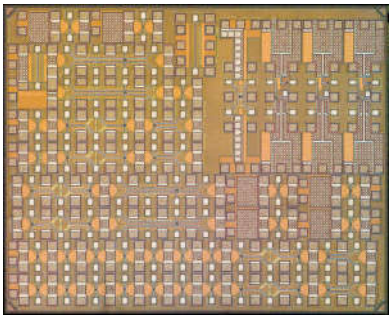

Fig. 1: Die microphotograph with chip dimensions of 2.5mm x 2.0mm. Included on die are 1x, 2x, and 3x pitch transistor test structures, passive components, quantum dot structures, and double quantum dot with readout circuits.

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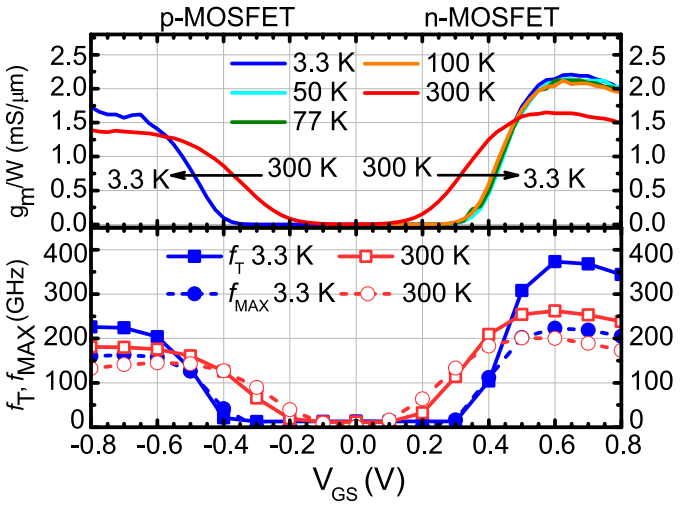

Fig. 2: Measurements for 40x20nmx590nm MOSFETs (V_{DS}=±0.8V) a) normalized transconductance b) f_T/f_{MAX} vs. V_{GS}

All transistor S-parameter measurements include parasitics of the wiring stack up to the top metal. The latter was designed to satisfy electromigration rules up to 110 °C. However, at 2-4 K, electromigration is not a problem and the wiring stack could be redesigned for significantly reduced parasitics, resulting in better circuit performance than reported here. Compared to 300 K, at 3.3 K the peak transconductance increases by 34% and 25% for the *n*- and *p*-MOSFET, respectively. Peak f_T improves by 42% (to 373 GHz) and 25% (to 226 GHz) for *n*-/*p*-MOSFETs, while peak f_{MAX} improves by about 11% to 223 GHz and 163 GHz, respectively. The peak-f_T, peak-f_{MAX} current densities remain nearly constant across temperature, simplifying the design of circuits that must operate over a wide temperature range, even in the absence of transistor models valid at 2-4 K.

Finally, Fig. 5 shows the measured characteristics of the transmission line, MOM capacitor, and poly-Si resistor at 3.3 K and 300 K. The 50Ω transmission line retains its characteristic impedance from room temperature (as evidenced by its measured S_{11}) and has lower loss at 3.3 K. The MOM capacitor Q improves at lower temperatures while the capacitance does not change. The poly-Si resistor retains the same resistance across temperature, which is again very important in designing transimpedance amplifiers (TIAs) whose output impedance does not change across temperatures.

III. Readout Amplifier Design

The fabricated qubit structures consist of minimum-size Si *n*-MOSFETs and SiGe *p*-MOSFETs and cascodes. QDs are formed in the thin (<10 nm) undoped semiconductor film below each top gate, which can be biased to control the confinement energies of each QD while the back gate formed in the Si substrate below the buried oxide layer controls the amount of coupling between the QDs in the cascode, which acts as a double quantum dot (DQD) [7]. The QD structures are expected to behave as electron- and hole-spin qubits when a DC magnetic field is applied [4]. Fig. 6 compares measured I-V transfer characteristics of electron- and hole-spin single quantum-dots at 2 K and 300 K. At 2 K and low V_{DS} bias

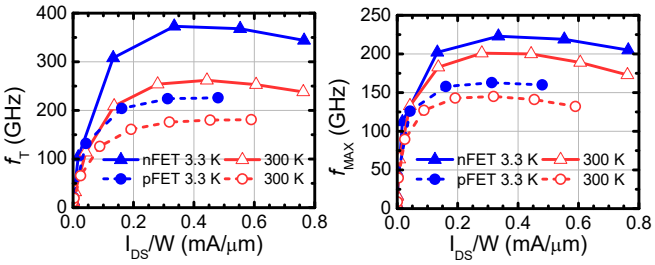

Fig. 3: Measured f_T *and* f_{MAX} vs. current density for 40x20nmx590nm MOSFETs (V_{DS}=±0.8V)

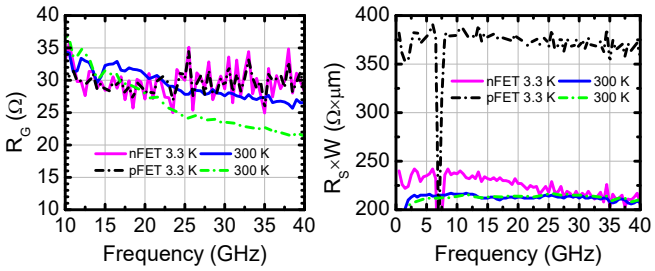

Fig. 4: Measured R_G, R_S for 40x20nmx430nm MOSFETs

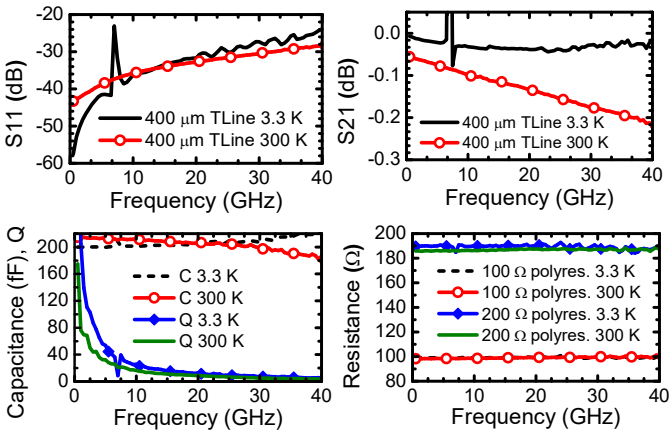

Fig. 5: Measured passives at 3.3 K and 300 K. a) 400μm long transmission line S_{11}, b) 400μm long transmission line S_{21}, c) 200fF MOM capacitor, and d) 100Ω and 200Ω poly resistors.

(<50mV), current oscillations are observed in the sub-threshold region, representative of electron/hole tunnelling events through the discrete energy levels of the QD. The TIA must detect the fast electron or hole charge transfer events and amplify the resulting small tunneling current at the first peak, on the order of 10 pA to 10 nA, to a voltage swing of at least a few mV, which can be easily processed by off-chip test equipment or FPGAs. This requires a low-noise, high-bandwidth readout amplifier with a transimpedance gain of 100-140 dBΩ, capable of driving 50 Ω without significantly loading the minimum-size QDs which have less than 60aF output capacitance. The circuit in Fig. 7 shows a DQD-with-TIA schematic, where the DQD is representative of a coupled-spin qubit when a DC magnetic field is applied. Both the TIA and the DQD are optimally biased, allowing qubit V_{DS} control through the V_{source} terminal and through the V_{DD} of the TIA. Figs. 8-9 show the measured output characteristics of the *n*- and *p*-MOSFET QDs when V_{GS} is set at the locations of the first peak and valley, respectively, as measured at 2 K in Fig. 6. For high fidelity, a QD with a large peak-to-valley current

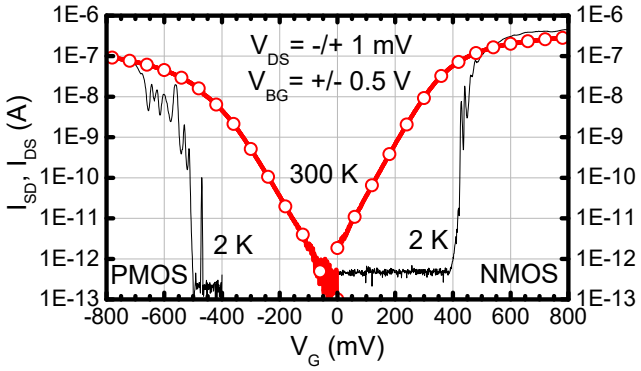

Fig. 6: Transfer characteristics at 2 K and 300 K for a 1x20nmx80nm *n*-MOSFET and *p*-MOSFET QD

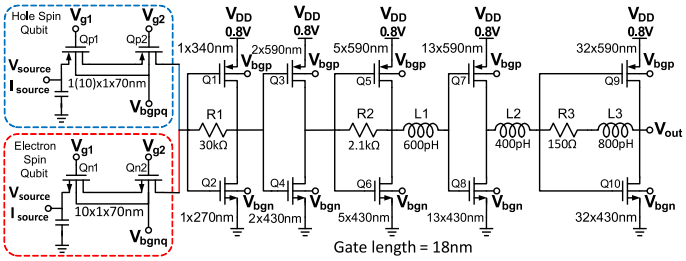

Fig. 7: Schematic diagram of integrated DQD structure and readout circuit

ratio, like the *p*-MOSFET in this 22nm FDSOI process, is desirable. In the *n*-MOSFET case, because of smaller source/drain barriers in the QD, the peaks and valley are observable in the transfer characteristics (Fig. 6) but reduce to plateaus in the output characteristics, Fig.8. In both cases, these characteristics show evidence of Coulomb blockade where the electrons/holes selectively tunnel out of the QD [7]. In the readout phase, precise V_{DS} values in the 0 mV to +/-5 mV range, are needed to scan for the first peak and valley in the output characteristics to ensure that the resulting drain tunneling current is from a single electron/hole.

To study the behaviour of both electron- and hole-spin qubits, 3 types of DQD structures were integrated with the same readout TIA: (i) a single finger *p*-MOSFET cascode (1x-DQD hole-spin qubit), (ii) a structure with ten *p*-MOSFET cascodes connected in parallel (10x-DQD hole-spin qubit) and, (iii) a structure with ten *n*-MOSFET cascodes connected in parallel (10x-DQD electron-spin qubit). All QD and TIA MOSFETs have a physical gate length of 18 nm. The QD gate finger width is 70 nm. Fig. 10 shows the layout for the QDs with 10 gate fingers connected in parallel. The readout amplifier consists of 3 cascaded CMOS-inverter TIA stages with CMOS inverters placed in-between to maximize gain. The interstage fanout is below 3 to maximize bandwidth. The MOSFETs and feedback resistor in the output stage were sized for 50Ω matching. To reduce noise, a large 30kΩ feedback resistor was used in the first TIA stage. To further minimize the noise and maximize gain, all MOSFETs are biased at the peak-f_{MAX} current density (J_{pfMAX} = 0.25 mA/μm) by adjusting the backgate voltages, V_{bgn} and V_{bgp}. The simulated transimpedance gain, bandwidth, and equivalent input noise current density at 2 GHz changes from 104 dBΩ, 12 GHz, 0.83 pA/√Hz to 112 dBΩ, 11 GHz, 0.19 pA/√Hz,

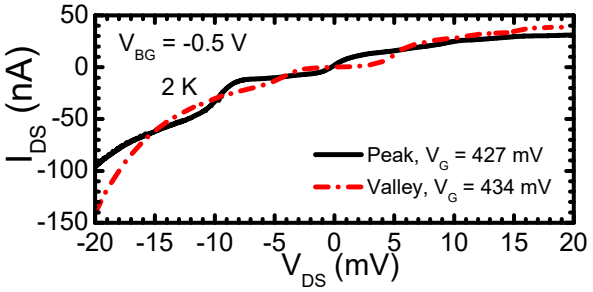

Fig. 8: Measured output characteristics at 2 K for the 1x20nmx80nm *n*-MOSFET QD from Fig. 6 when V_{GS} is set at the first peak and valley of the transfer characteristics in Fig. 6

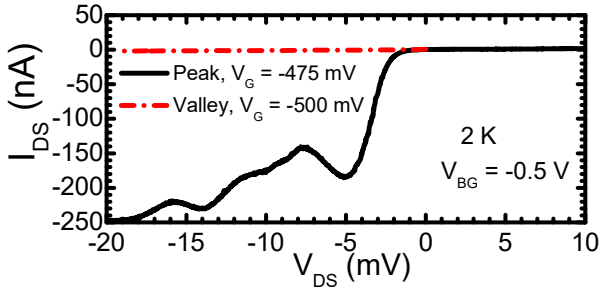

Fig. 9: Measured output characteristics at 2 K for the 1x20nmx80nm *p*-MOSFET QD from Fig. 6 when V_{GS} is set at the first peak and valley of the transfer characteristics in Fig. 6

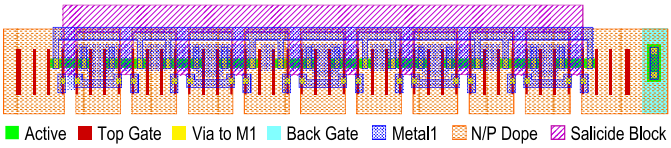

Fig. 10: Layout of integrated qubit structure with ten 1x18nmx70nm cascodes connected in parallel (10x)

respectively as the temperature decreases from 300 K to 12 K, the lowest at which the circuit simulator still works. The bandwidth of the TIA, 12 GHz, is designed to cover DC to 4x Rabi frequency when the DQD gate is excited with a mm-wave signal of up to 20 mV_{pp} in the 60-220 GHz range [7].

IV. Readout Amplifier Measurements

Fig. 11 compiles the measured S_{21} and S_{22} of all three DQD-with-TIA circuits at 300 K. Although, because of their small size and g_m, the standalone DQDs have an S_{21} of -20 dB or less, the 10x *n*-MOS DQD with TIA achieved a maximum S_{21} of 18.9 dB and a 3dB bandwidth of 7.5 GHz. The equivalent 10x *p*-MOS DQD with TIA readout circuit has an S_{21} of 13.5 dB and 7.5GHz bandwidth, while the 1x *p*-MOS DQD circuit reached a maximum S_{21} of 8.89 dB with a 3dB bandwidth of 8.5 GHz. In all 3 versions, S_{22} is better than -10 dB up to 60 GHz. As in the transistor measurements in Fig. 3 and in our previous 3-stage readout TIA [7], it is expected that the gain and bandwidth will improve at 2 K, while the output will remain matched. Because a standalone 5-stage TIA was not fabricated in this run, the transimpedance gain, Z_{21}, of the readout amplifier itself was obtained by applying a variable DC current, I_{source}, through the V_{source} terminal and measuring the output voltage of the TIA, V_{out}, and its derivative, as reproduced in Fig. 12. The current was swept from -40 nA to +40 nA, covering the range of the DQD's tunnelling current.

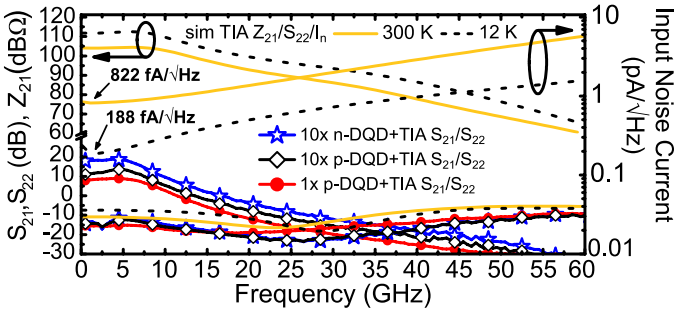

Fig. 11: Measured S-parameters of the integrated DQD-with-TIA circuits at 300 K, and simulated Z_{21}, S_{22}, and equivalent input noise current, I_n, of the TIA at 300 K and 12 K

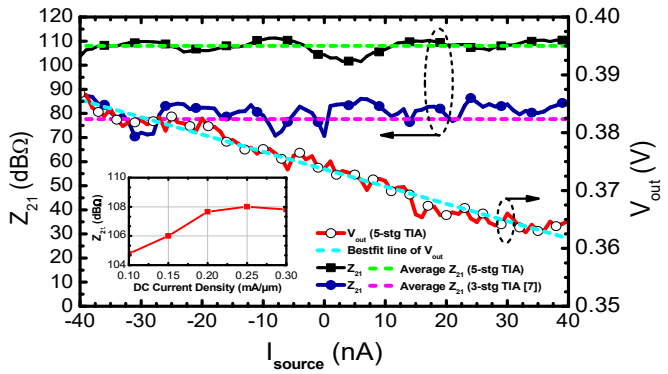

Fig. 12: Measured readout amplifier at 300 K showing Z_{21} from 1x *p*-MOS DQD plus amplifier circuits with inset showing Z_{21} as a function of TIA MOSFET drain current density

The peak Z_{21} is 108 dBΩ (251 kΩ) at a current density of 0.25 mA/μm, corresponding to J_{pfMAX}, as illustrated in the inset of Fig. 12. The output spectrum of the 1x p-DQD with TIA was measured with variable-amplitude sinusoidal signals in the 1-8GHz range applied to the gate of the DQD. Fig. 13 shows that even at -110dBm output power, the 4GHz sinusoidal signal is clearly visible above the noise floor. Based on the 251 kΩ TIA gain, this corresponds to $3pA_{rms}$ current at the input of the TIA. Table 1 compares the performance of the DQD with TIA to other state-of-the-art qubit readout amplifiers intended to operate at cryogenic temperatures.

V. Conclusion

The measured DC transfer and output characteristics of electron and hole single and double quantum dots at cryogenic temperatures were taken into consideration in the design of a readout TIA which was monolithically integrated with single and multi-finger DQD qubit structures in a production 22nm FDSOI CMOS process. Unlike in other applications, this TIA was optimized to read qubit currents in the range of 10 pA and 10 nA with ultra-low input capacitance to avoid overloading the qubits and to maximize the spin-readout bandwidth. Transistor measurements show that most of the performance and V_t variation occur between 300 K and 100 K. The high frequency performance improves at 3.3 K compared to 300 K while the peak f_T and f_{MAX} current densities remained unchanged. Combined with the fact that the quality factor of the passive components also improves, while their values remain practically unchanged at cryogenic temperatures, this makes it possible to reliably design all the readout and control

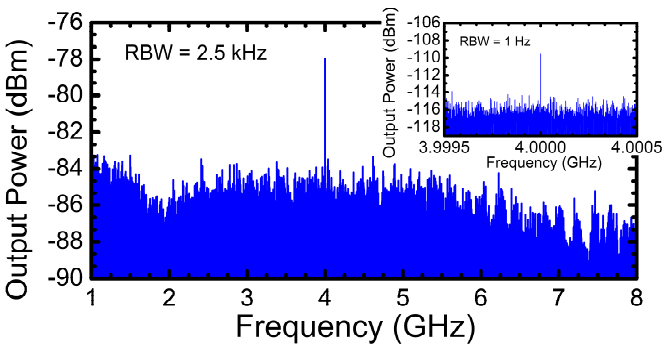

Fig. 13: Measured output spectrum of the 1x *p*-DQD with TIA at 300 K showing a -78dBm output signal (corresponding to $120pA_{rms}$ TIA input current) at 4 GHz and, in the inset, a -110dBm output signal (corresponding to $3pA_{rms}$ TIA input current) also at 4 GHz on a zoomed-in scale

Table 1: Comparison of state-of-the-art qubit readout amplifiers

Parameter	10x n-DQD with TIA	TIA only [7]	LNA [8]
Technology	22nm FDSOI	22nm FDSOI	160nm Bulk
S_{21} (dB)	19 @ 300 K	15/20 @ 300/2 K	57 @ 4 K
BW (GHz)	7.5 @ 300 K	4/5 @ 300/2 K	0.5 @ 4 K
$Z_{21,TIA}$ (dBΩ)	108/112 @ 300/12* K	78/80 @ 300/2 K	N/A
P_{DC} (mW)	4.5 @ 300 K	3.1 @ 300/2 K	45.9 @ 4 K

*simulated

electronics in a FDSOI CMOS monolithic quantum processor using standard design kit models, calibrated down to 100 K. The 4.5mW TIA power consumption allows for monolithic integration of up to 440 qubits with individual readout amplifiers within a power budget of 2 W. This dissipated power can be removed with state-of-the-art cryostats at 4 K.

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