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A DC to 220-GHz High-Isolation SPST Switch in 22-nm FDSOI CMOS

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***Abstract*—A wideband single-pole single-throw (SPST) switch covering the dc to 220-GHz frequency range is presented in this letter. A four-element distributed topology is used to extend operation to the upper millimeter-wave band. With a combination of front-gate and back-gate biasing, unique to fully depleted silicon-on-insulator (FDSOI) MOSFETs, and enabled by the thick metal/dielectric backend of the technology, the switch achieves an insertion loss of 3.1 dB and an isolation of 37 dB at 220 GHz, as well as a peak isolation of 58 dB at 200 GHz, without deembedding the pads. A *G*-band variable gain low-noise amplifier featuring the SPST switch shows >50-dB gain control range, with a maximum peak gain of 9.5 dB at 190 GHz and a 3-dB bandwidth from 180 to 203 GHz.**

***Index Terms*—Fully depleted silicon-on-insulator (FDSOI) CMOS, isolation, LNA, millimeter-wave (mm-wave), single-pole single-throw (SPST) switch, variable gain.**

I. Introduction

FULLY depleted silicon-on-insulator (FDSOI) CMOS is a promising candidate for the realization of monolithically integrated quantum processors (QPs) based on spin qubits [1], [2]. Coherent spin manipulation requires the pulsing of a millimeter-wave (mm-wave) signal, with the on–off ratio of the resulting burst directly translating into the gate fidelity of the qubit. The on-chip generation of such a qubit control signal requires a high-isolation single-pole single-throw (SPST) switch, as shown in Fig. 1. High-performance switches are also key components of conventional RF front-ends. Notably, the single-pole double-throw (SPDT) switch performs transmit/receive duplexing functions in today's wireless systems. The SPST switch, as a building block of SPDT antenna switches, must in turn adhere to stringent low insertion loss and high isolation requirements.

In this letter, we demonstrate a SPST switch implemented in 22-nm FDSOI CMOS that covers the entire dc-220 GHz range with <3.1-dB insertion loss and >37-dB isolation above 60 GHz. The switch was also integrated into a 200-GHz variable gain LNA (VGLNA) both to better characterize its isolation and as an emulation of the front-end of the proposed elevated temperature (4–12 K) monolithic QP [1], where

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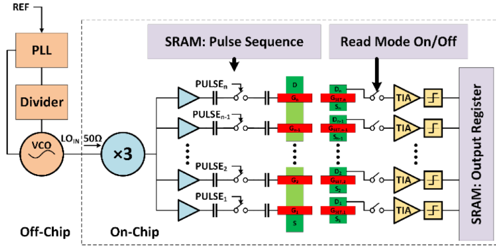

Fig. 1. Proposed mm-wave monolithic QP.

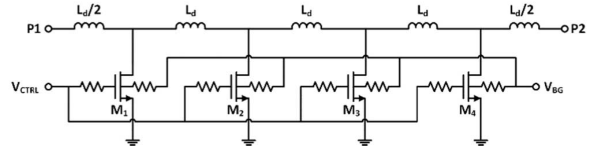

Fig. 2. Schematic of the proposed distributed SPST switch.

switch isolation of >40 dB is required for 10^{-4} error rates. In spin qubit QPs, the operation temperature scales linearly with the spin manipulation frequency [1], for example, ~40 GHz was needed for 1.5 K operation [3].

II. Distributed SPST Switch Design

The schematic of the proposed distributed SPST switch is shown in Fig. 2. It is composed of four evenly sized shunt super low V_t (SLVT) n-MOSFETs, connected at their drains by high-impedance microstrip lines. In the OFF-state, the signal path is shorted to ground via the ON-state resistance, R_{ON}, of the shunt MOSFETs. In the ON-state, the MOSFETs are off, and the OFF-state capacitance, C_{OFF}, of the individual transistors is absorbed into a distributed T network. An artificial transmission line is thus created, allowing the SPST switch to operate over a wideband, through the higher mm-wave frequencies. The microstrip lines are modeled here by a lumped inductance, L_d, with parasitic capacitances, C_d, to ground on both ends. The characteristic impedance of the ON-state artificial transmission line is then given by

$$Z_0 = \sqrt{\frac{L_d}{(C_{OFF} + 2C_d)}}. \quad (1)$$

The size of the unit shunt transistor and the number of switch stages are the most critical parameters in the design of a high-isolation SPST switch. Increasing the gate width of the individual transistor, needed for improved isolation, leads to large C_{OFF}, reducing the bandwidth. Increasing the number of stages becomes the preferred approach. A four-stage design is adopted here because it presents significant improvements

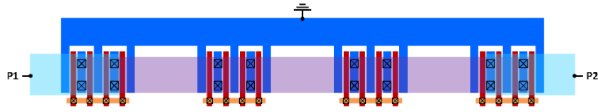

Fig. 3. Not-to-scale layout implementation of the SPST switch. The five higher metal microstrip lines are fused into three main sections (cyan and purple) overtop the four shunt switch transistor drains. The "x" symbols represent via connections between overlapping metal layers.

in isolation compared with its three-stage counterpart [4]. The final unit transistor has a gate width of 44 × 900 nm and a gate length of 18 nm. Gate- and body-floating resistors of 12.5 kΩ are added to reduce C_{OFF}. The resulting unit switch has a simulated postextraction C_{OFF} of 12 fF and R_{ON} of 9.1 Ω at $V_{\mathrm{GS}} = 0$ and 0.8 V, respectively, with $V_{\mathrm{BG}} = 0$ V. The linear back-gate threshold voltage control, unique to FDSOI [5], can be exploited in conjunction with conventional front-gate biasing to improve the switch performance. By setting $V_{\mathrm{GS}} = -0.8$ V, as in [6], and $V_{\mathrm{BG}} = 0$ V, the insertion loss is minimized, while the isolation is maximized with $V_{\mathrm{GS}} = 0.8$ V and $V_{\mathrm{BG}} = 4$ V, due to further reduced C_{OFF} and R_{ON}, respectively.

The microstrip lines are designed so that $L_d = 36$ pH to yield an SPST switch ON-state Z_0 close to 50 Ω. They are formed in either the top aluminum layer or the highest copper layer over a metal 1 ground plane and set to the minimum allowed width. The microstrip lines are routed directly atop the shunt transistors, thus eliminating lateral metal connections and minimizing the parasitic capacitance from the mm-wave signal path to ground. A layout detail of the switch is shown in Fig. 3.

III. 200-GHz VGLNA Design

The measured MAG of 22-nm FDSOI n-MOSFETs wired up to the top metal is <2 dB at 200 GHz. Therefore, cascode stages were used in the LNA to provide an additional 2 dB of gain per stage. The transistor size was chosen to ensure that the optimal noise impedance is matched to the source impedance at 200 GHz. SLVT n-MOSFETs with 18-nm gate length and 30 × 430 nm wide gate fingers contacted on both sides of the gate were selected to minimize $\mathrm{NF}_{\min}$ of the first stage. Given the reduced MAG at 200 GHz, all stages were made identical to minimize the overall noise figure of the LNA. The schematic of the three-stage VGLNA is shown in Fig. 4. The cascodes are biased through a resistive divider from the 1.6-V power supply, which ensures that V_{GS} of the common-gate MOSFET and its drain current density are identical to those of the common-source device. Not shown in the schematic is an additional back-gate biasing resistive divider used to control the bias current density of the LNA. The back-gate voltage can be set to achieve an optimum noise current density of 200 μA/μm or, alternatively, to bias all the stages at the maximum gain current density of 300 μA/μm and thus maximize power gain. The SPST switch is connected at the output of the LNA, providing on/off and variable gain control. The switch consumes no dc power.

IV. Experimental Results

The SPST switch and VGLNA were fabricated in GlobalFoundries' 22-nm FDSOI CMOS process with mm-wave back end of line (BEOL). The die micrographs of the SPST switch and VGLNA are shown in Fig. 5. The die area

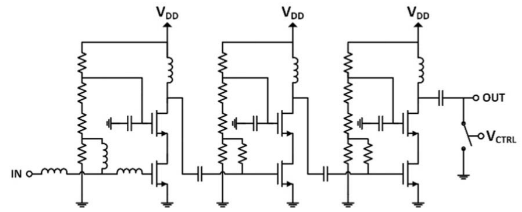

Fig. 4. Schematic of the VGLNA.

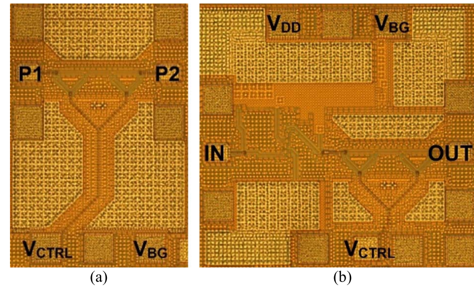

Fig. 5. Die micrographs of (a) SPST switch breakout and (b) VGLNA breakout.

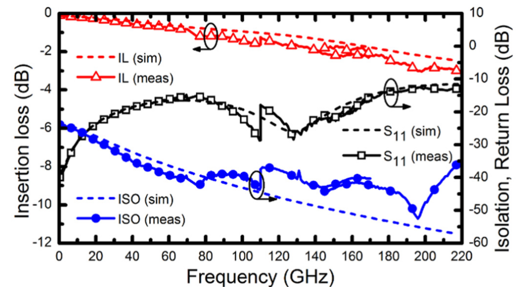

Fig. 6. Measured versus simulated insertion loss, return loss, and isolation of the SPST switch.

of the SPST switch is 330 μm × 495 μm, with a core of 225 μm × 115 μm. The die area of the VGLNA is 515 μm × 480 μm. The circuits were tested on die.

A. SPST Switch

The SPST switch was characterized over four frequency bands from dc to 220 GHz. The dc-to-67 GHz, W-band, D-band, and G-band S-parameters were measured separately using either the Keysight N5227A vector network analyzer (VNA) or the Agilent 8150C VNA paired with the appropriate Oleson or Virginia Diodes mm-wave extenders, where applicable. In each frequency band, calibration was performed up to the probe tips with the line-reflect-reflect-match (LRRM) method using calibration standards on an alumina impedance standard substrate (ISS). The on-die pads were not deembedded from the measurement results, as they are part of the circuit. The measured pad Q is less than 10 above 100 GHz and can be modeled as a 5-fF capacitance in series with a 50-Ω resistance.

Fig. 6 compares the measured and simulated insertion loss at $V_{\mathrm{GS}} = -0.8$ V and $V_{\mathrm{BG}} = 0$ V and the isolation at $V_{\mathrm{GS}} = 0.8$ V and $V_{\mathrm{BG}} = 4$ V. The insertion loss is 1.6 dB at 110 GHz and 3.1 dB at 220 GHz, while the return loss remains better than 12 dB up to 220 GHz. There is a 0.3-dB improvement

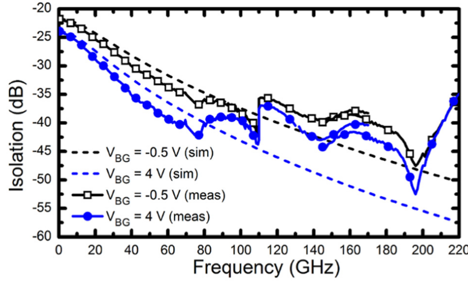

Fig. 7. Measured versus simulated isolation of the SPST switch with the back-gate voltage swept at −0.5 and 4 V.

TABLE I
MEASURED SWITCH PARAMETERS

Parameter	@V_{BG} = -0.5 V	@V_{BG} = 4 V
C_{gs} @V_{GS} = 0 V	0.40 fF/µm	0.49 fF/µm
C_{gd} @V_{GS} = 0 V	0.38 fF/µm	0.47 fF/µm
C_{ds} @V_{GS} = 0 V	0.33 fF/µm	0.15 fF/µm
R_s @V_{GS} = 0.8 V	167 Ω×µm	122 Ω×µm

Measurements for a 40×18nm×590nm SLVT n-MOSFET at V_{DS} = 1 mV

in insertion loss at 220 GHz when V_{GS} is changed from 0 to −0.8 V because of the reduction in C_{OFF}. A further 0.3-dB improvement in insertion loss is obtained at 220 GHz if the pads are deembedded. The variation in insertion loss across eight dies remains <0.34 dB up to 220 GHz. By changing V_{BG} from 0 to 4 V, the isolation is improved by 2–4 dB throughout the entire range up to 220 GHz. The agreement between measurements and simulation is excellent up to 67 GHz (the range in which the transistor models were extracted) and remains acceptable up to 220 GHz. It should be noted that the measurement of isolation values better than 40 dB is limited by the noise floor of the VNA setup above 110 GHz, and that isolation was not calibrated during the LRRM calibration method. Since the gain of the LNA improves the measurement dynamic range, the true switch isolation is obtained at the G-band from the measured S_{21} of the VGLNA when the switch is turned on and off. The directly measured and simulated G-band isolation at $V_{GS} = 0.8$ V for $V_{BG} = -0.5$ and 4 V are shown in Fig. 7. As V_{BG} increases, R_{ON} decreases and the capacitances increase, improving isolation. Indeed, a 40 × 18 nm × 590-nm SLVT n-MOSFET fabricated on the same die and biased as a switch in triode at V_{DS} = 1 mV exhibits different measured C_{gs}, C_{gd}, C_{ds}, and R_{ON} as the back-gate bias voltage is varied. Table I compiles the measured switch parameters of the SLVT n-MOSFET. Table II compares the performance of the SPST switch with the state-of-the-art wideband switches in CMOS and SiGe BiCMOS technologies. This work achieves the best isolation by far and similar bandwidth as the 45-nm partially depleted silicon-on-insulator (PDSOI) switch [8], with 1.6 dB higher loss at 220 GHz.

B. 200-GHz VGLNA

Fig. 8 shows the measured and simulated S-parameters of the VGLNA in the 170–220-GHz range. The VGLNA exhibits a peak gain of 9.5 dB at $V_{DD} = 1.8$ V (0.8 dB higher than at $V_{DD} = 1.6$ V), centered at 190 GHz with a 3-dB bandwidth of 23 GHz, ranging from 180 to 203 GHz, when the switch is off and biased for minimum insertion loss at $V_{GS} = -0.8$ V and $V_{BG} = 0$ V. The LNA was biased for maximum gain to

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART SWITCHES

Ref.	[7]	[8]	[9]	[10]	This work
Type	SPDT	SPST	SPST	SPDT	SPST
Tech	90nm CMOS	45nm SOI CMOS	90nm SiGe BiCMOS PIN diode	130nm SiGe HBT	22nm FDSOI CMOS
Freq (GHz)	dc - 110	dc - 220	dc - 125	dc - 110	dc - 220
IL (dB)	< 5.5	≤ 1.5	< 3.6	≤ 3.0	< 3.1
ISO (dB)	> 40	20 @220GHz	22 @160GHz	27.3 @60GHz	58** @200GHz > 37 dB** 60-220GHz
RL (dB)	> 10	> 10	≥ 10	> 10.9	> 12
Area (mm^2)	0.067*	0.203	0.106	0.098*	0.026*

* core area, ** from VGLNA S_{21} measurements

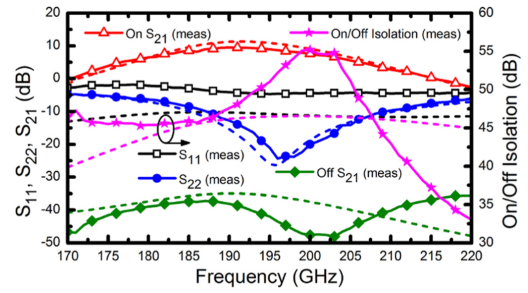

Fig. 8. Measured versus simulated S-parameters of the VGLNA.

characterize switch isolation, drawing a total of 13.1 mA from 1.8 V for a total power consumption of 23.5 mW. Based on the measured loss of the switch breakout, the gain of the LNA itself is estimated to be 12 dB. Also shown is the measured and simulated attenuation of the VGLNA when the switch is off, at $V_{GS} = 0.8$ V and $V_{BG} = 0$ V. Subtracting the maximum attenuation from the maximum VGLNA gain gives a gain control range of >45 dB over 170–208 GHz, and >50 dB between 194 and 205 GHz, with a peak value of 55.2 dB at 200 GHz. These numbers also correspond to the on–off ratio of the switch. Another 3–4 dB of improvement in on–off ratio is expected if V_{BG} of the switch is set to 4 V, as shown in Fig. 7. However, this was not possible in the VGLNA breakout since the switch back-gate was hardwired to ground.

V. CONCLUSION

A wideband SPST switch operating from dc to 220 GHz and optimized for quantum computing applications requiring >40-dB isolation above 60 GHz was demonstrated and integrated with a 200-GHz VGLNA, as needed for spin manipulation in an elevated temperature QP with spin resonance frequencies around 200 GHz and operation temperatures up to 10 K. To the best of the authors' knowledge, these results mark the highest frequency switch and LNA reported to date in sub-28-nm CMOS technologies and the highest isolation switch above 60 GHz in any technology. The >50-dB isolation around 200 GHz suggests that spin manipulation of qubit gates with $<10^{-5}$ error rates is possible.

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