A 210–284-GHz I–Q Receiver With On-Chip VCO and Divider Chain

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***Abstract*— A 240-GHz direct conversion I–Q receiver with 74-GHz RF bandwidth is reported. It features a mixer-first architecture with fundamental local oscillator (LO)-frequency Gilbert-cell downconversion mixers, variable-gain baseband amplifiers, and a 240-GHz LO source, making it the first fully integrated 240-GHz I–Q receiver. With a phase noise of −82 dBc/Hz at 1-MHz offset, the LO source has a 27-GHz tuning range and consists of a 120-GHz voltage-controlled oscillator (VCO), a frequency doubler, and a static divide-by-128 chain. The measured peak downconversion gain is 23 dB and is adjustable over 38 dB. Along with the IF bandwidth of 59 GHz, the wide RF bandwidth makes it suitable for both high data-rate communication and emerging quantum computing applications. The chip occupies an area of 1.837 mm^2 and consumes 859 mW.**

***Index Terms*— 90° hybrid coupler, divider, I–Q downconverter, receiver, SiGe BiCMOS, variable-gain amplifier (VGA), voltage-controlled oscillator (VCO).**

I. Introduction

With the continued improvement in the high-frequency performance of SiGe HBTs and SiGe BiCMOS technologies, the 200–300-GHz band has become attractive for higher data-rate communication transceivers [1]. Recent publications also report significantly improved high-frequency performance of advanced SiGe HBTs [2] at cryogenic temperatures compared with 300 K. Early measurements of HBTs used in this letter also indicate large improvement (see Fig. 1). This opens up the prospect of such wideband communication receivers to also be used in the dispersive readout of emerging cryogenic quantum computers [3]–[5]. The larger available bandwidth in the 200-GHz band would allow higher qubit integration through frequency-division multiplexing (FDM) [4] and to increase the operating temperature to 4–12 K due to improved immunity to thermal noise [6]. Therefore, it is important to demonstrate highly integrated complex receivers and transceivers, which also satisfy the more stringent criteria for signal isolation, and system integration of potentially thousands of qubits and of their associated mm-wave control and readout paths. This letter describes the first I–Q receiver with integrated local oscillator (LO) generation, covering the 210–284-GHz band for high data-rate wireless communication systems and which is also suitable for prospective large-scale quantum processors.

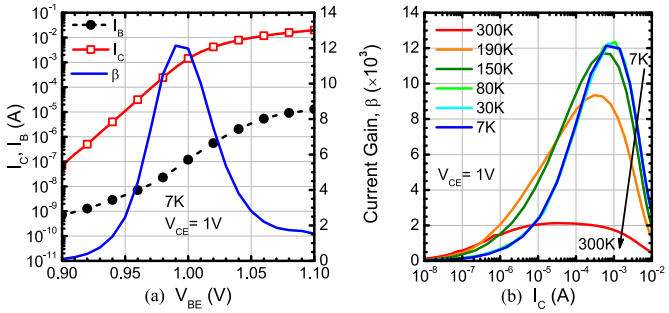

Fig. 1. Measured 0.1 × 4.5 µm SiGe HBT. (a) Gummel plot at 7 K. (b) Current gain β versus collector current across temperature.

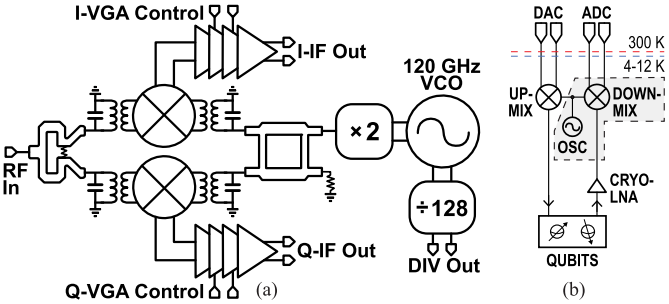

Fig. 2. (a) Block diagram of the receiver and (b) its possible application in an integrated quantum processor [3], [5].

II. System Architecture

Fig. 2(a) shows the block diagram of the proposed SiGe BiCMOS direct conversion, mixer-first I–Q receiver. Since the room temperature f_T = 320 GHz and f_{max} = 370 GHz of the SiGe HBTs in the available technology [7] are only slightly above the intended frequency range of the receiver and the HBT minimum noise figure NF_{min} is larger than its maximum-available gain (MAG), in this band, an LNA is not used. It would make it more challenging to achieve a wide RF bandwidth design without providing significant gain and noise figure improvement. This tradeoff will improve when scaled SiGe HBTs with f_{max} = 700 GHz [8] become available. For this letter, the RF path is simplified where the external signal passes through a low-loss ultrabroadband Wilkinson power splitter and is then converted to differential format by lumped transformers before it is fed to the two downconverters. The

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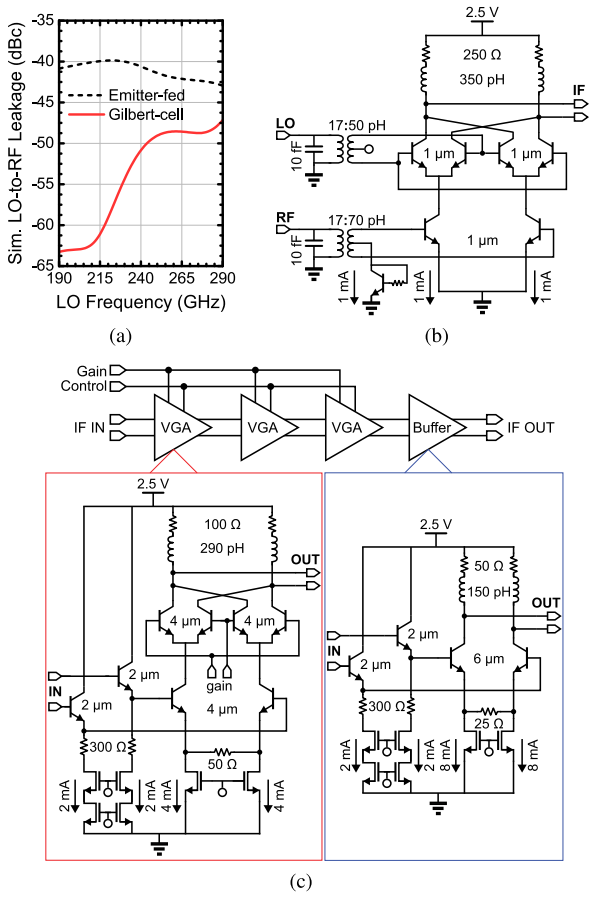


Fig. 3. (a) Simulation comparison of LO-to-RF leakage of Gilbert-cell and emitter-fed mixers. Schematics of (b) double-balanced Gilbert-cell downconversion mixer and (c) IF VGA chain with 50-Ω output buffer.

transconductors in each downconverter are sized and biased to also act as low-noise amplifiers at 200–300 GHz.

The LO signal is generated on-chip using a 120-GHz Colpitts voltage-controlled oscillator (VCO) followed by a doubler. The VCO also drives a static divider chain, which provides an output signal at around 1 GHz and can be used to lock the LO source with an external 1-GHz phased-locked loop (PLL), as in [9]. The design and performance of the LO generation and the divider chain were described in [10]. The doubler output signal is applied to a 90° hybrid coupler and transformers for single-ended-to-differential conversion. All the passive components were modeled with the EMX 2.5-D electromagnetic field simulator. The measured I–Q amplitude and the phase imbalance of a breakout of the hybrid coupler are below 0.6 dB and 4°, respectively, and the insertion loss is lower than 1.5 dB in the 230–250-GHz range.

This LO signal source architecture was preferred over longer multiplication chains, as it provides higher output power with high efficiency and much fewer spurs, very important in broadband FDM systems such as those used in quantum processors [10]. The output power of the signal source is more important in large integrated systems where it must drive many I–Q receiver and transmitter chains, and where the LO distribution becomes extremely challenging, especially at 240 GHz. Following the downconverter, linear, ultrawideband variable-gain IF amplifiers are used to compensate for any I–Q amplitude imbalance and adjust the signal level for downstream analog-to-digital convertors (ADCs).

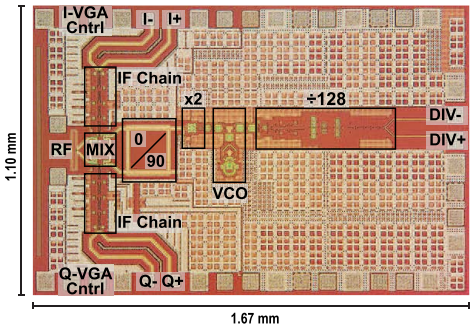


Fig. 4. Die micrograph.

III. Circuit Design

In a mixer-first architecture, the LO-to-RF leakage becomes an issue, especially for quantum computing applications where undesired tones can cause dephasing of qubit states. Fig. 3(a) shows a simulation comparison of the LO-to-RF leakage between the double-balanced Gilbert-cell topology used in this letter [see Fig. 3(b)] and an emitter-fed mixer, as in [1] and [11]. The Gilbert-cell mixer was chosen because of its improved isolation and conversion gain (CG). The RF transconductor stage is biased near the minimum noise current density through a current mirror connected to the transformer center tap. This bias scheme maximizes V_{CE} and MAG of the HBTs and avoids $1/f$ noise, which would have been problematic if polysilicon resistors were used in the bias network. In this technology, the optimal noise resistance (R_{sopt}) of the HBT and its input resistance (R_{in}) are almost identical at 240 GHz. This simplifies the simultaneous noise and impedance matching methodology in [12], without the need for an emitter degeneration inductor, thus maximizing gain. R_{in} and R_{sopt} are simultaneously matched to 50 Ω through a transformer. However, both the HBT and the transformer size need to be carefully codesigned at these frequencies. A secondary (L_2)-to-primary-inductance (L_1) ratio larger than 4 is difficult to realize with a reasonable magnetic coupling factor. In addition, L_2 must be kept below 100 pH so that its self-resonance frequency is higher than the operating frequency. Keeping the HBT size as large as possible, while resonating its input capacitance out with L_2, maximizes the downconversion gain.

Fig. 3(c) shows the schematic of the IF variable-gain amplifier (VGA) chain. The three identical cascaded VGA stages consist of an emitter follower (EF) and a current steered Gilbert-cell multiplier biased at the peak-f_T current density for maximum bandwidth. To prevent instability due to negative resistance, the EF stages are connected through very short lines to the Gilbert-cells, and 300-Ω resistive padding is inserted between the EF and its current source. MiM capacitors are also added at the base of the common base transistors in the Gilbert-cells to ensure stability. To minimize the supply voltage and power consumption, differential emitter degeneration resistors are used for linearization in each variable-gain cell. A 50-Ω output buffer was also added to achieve wideband output matching. Harmonic balance ac simulation shows that the mixer has a voltage CG of 2 dB, while the IF amplifier chain has a voltage gain of 27 dB.

IV. Experimental Results

The circuit was fabricated in a 55-nm SiGe BiCMOS technology with nine metal layers, MiM capacitors, 55-nm MOSFETs with high-, standard-, and low-V_t, and SiGe HBTs

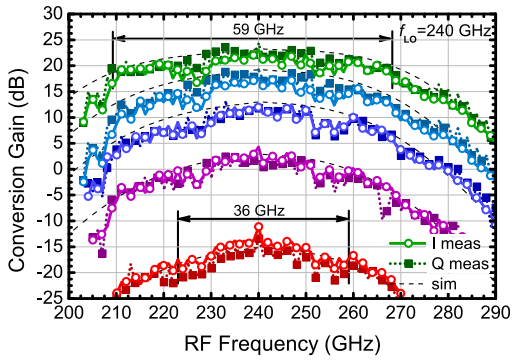


Fig. 5. CG as a function of the RF frequency for different gain settings (f_{LO} = 240 GHz).

TABLE I

COMPARISON OF RECENTLY PUBLISHED 240-GHZ RECEIVERS

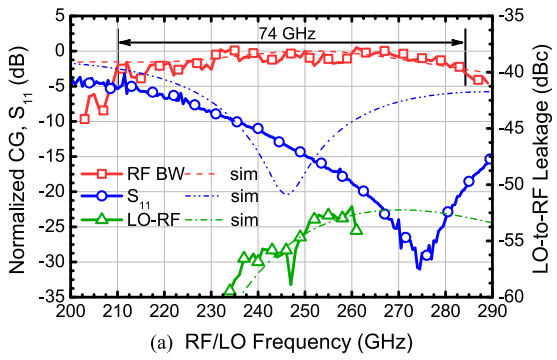
	This work	[1]	[11]	[13]	[14]
Technology	**55-nm SiGe**	130-nm SiGe	130-nm SiGe	130-nm SiGe	65-nm CMOS
f_T/f_{max} (GHz)	**320/370**	300/500	350/550	300/500	–
Frequency (GHz)	**240**	240	240	245	240
LO Architecture	**VCO + ×2, ÷128**	×8	×16	–	ILO + ×3
IF, RF BW (GHz)	**59, 74**	55, –	24, 47	25, –	14, –
CG (dB)	**23 → -15**	32 → 7	11.3	18 → -18	25
IP_{1dB} (dBm)	**-27.3**	-28.5	–	-27	–
NF (dB)	**24.5**	13.4	11.3	18 (sim.)	15 (sim.)
LO-RF Leak. (dBc)	**-56**	-30	–	–	–
Area (mm^2)	**1.837**	4.5	1.256	2.3	2
DC (mW)	**859 (293*)**	575	915.8	512.5	260

*DC consumption excluding LO & divider chain

with f_T/f_{max} of 320/370 GHz [7]. The die micrograph is shown in Fig. 4 and occupies an area of 1.67 mm × 1.10 mm.

To cover its entire bandwidth, the receiver performance was measured using both 140–220-GHz and 220–325-GHz signal sources from the vector network analyzer (VNA) extenders, using WR-5 and WR-3 GSG probes, respectively, at the RF port. The output power of the VNA frequency extenders was characterized with an Erickson calorimeter. The IF output power and the frequency of the receiver were monitored on a 50-GHz spectrum analyzer. The CG and the IF bandwidth shown in Fig. 5 were obtained with the VCO frequency set to 240 GHz, as f_{RF} was swept. A maximum CG of 23 dB with an IF bandwidth of 59 GHz were achieved. The gain control range is 38 dB. Due to the relatively limited tuning range of the VCO, of only 27 GHz, the RF bandwidth, as shown in Fig. 6(a), was characterized by measuring the CG at multiple fixed IF frequencies, while f_{RF} was swept. From these data, the IF bandwidth was deembedded and a normalized CG with 74-GHz bandwidth was obtained. The measured input return loss is better than −5 dB from 200 to 300 GHz, with the best return loss of −30 dB centered on 275 GHz. The measured LO-to-RF leakage was better than −52 dBc across the 234–261-GHz VCO tuning range from the output of the doubler to the RF pad.

The receiver noise figure was estimated with the gain method by measuring the noise power at a single-ended IF output. A double-sideband (DSB) noise figure of 24.5 dB was obtained for most of the RF bandwidth, as shown in Fig. 6(b). This value includes the noise of both I and Q mixers and the 3-dB signal division of the ideal Wilkinson power splitter.



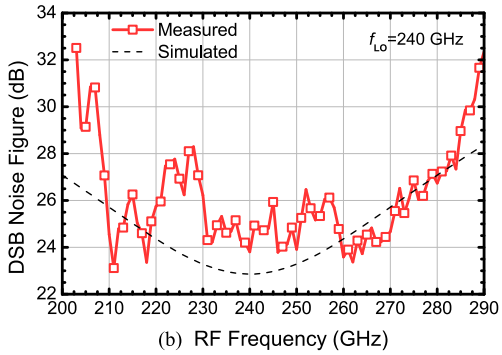


Fig. 6. (a) RF bandwidth, input return loss, and LO-to-RF leakage. (b) DSB noise figure versus RF frequency at the highest gain setting.

The overall system noise figure improves by 6 dB when the I and Q outputs are combined for upper- and lower-sideband selection and when accounting for the differential output. Noise summary simulation shows the input Wilkinson divider and RF balun, the mixer, the first IF amplifier stage, and other circuitry contributing 0.9%, 84.6%, 13%, and 1.5% of the total receiver noise, respectively.

The 1-dB compression point ($IP_{1\,dB}$) was characterized at different gain settings for an RF signal of 220 GHz (f_{IF} = 20 GHz) using the 140–220-GHz VNA frequency extender due to its higher output power. The measured $IP_{1\,dB}$ was −27.3 and −11 dBm at the highest and medium gain settings, respectively.

V. CONCLUSION

A mixer-first I–Q receiver with an integrated LO source and divider chain was demonstrated over the 210–284-GHz range. A comparison of its performance with state-of-the-art radio receivers is compiled in Table I. The record RF and IF bandwidths of 74 and 59 GHz, respectively, make this circuit suitable for high data-rate communication. A potentially new application is also in large-scale quantum processors, which would take advantage of the high spin resonance frequencies and FDM to operate at 4–12 K. Cryogenic operation is expected to significantly improve the minimum noise figure f_T and f_{max} of the SiGe HBTs used in this letter, which would further improve the receiver performance. The low power consumption makes it suitable for cryogenic operation and future monolithic integration with Si/SiGe qubits.

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