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Compact Modelling of 22nm FDSOI CMOS Semiconductor Quantum Dot Cryogenic I-V Characteristics

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***Abstract*— A compact analytical model is reported capturing the effects of Coulomb Blockade and charge quantization on the drain current characteristics of a MOSFET-based semiconductor quantum dot at cryogenic temperatures. It is implemented as a Verilog-A add-on to the foundry-provided MOSFET model to facilitate potential integration in any design kit and allow for simulation of quantum processors that integrate qubits and control electronics on the same die. The model was verified in the 6-50 K temperature range on the measured I-V characteristics of a nanoscale p-MOSFET fabricated in production 22nm FDSOI CMOS technology.**

Keywords—compact modelling, Coulomb Blockade, cryogenics, semiconductor quantum dot, silicon germanium, silicon-on-insulator

I. INTRODUCTION

The modelling of the classical behaviour of MOSFETs at cryogenic temperatures [1][2] has garnered recent interest due to their application in the classical control and readout electronics in superconducting- and semiconductor qubit quantum processors [3] – [5]. However, in commercial nanoscale CMOS processes, a quantum dot (QD) is formed in the channel of the MOSFET below the gate, separated from the source and drain contact regions by potential barriers below the gate oxide spacers [6]. This gives rise to strong quantum phenomena in the subthreshold characteristics at low temperature and small drain-source voltages, V_{DS}, [7] – [10] which have yet to be captured in design-kit models or the prior work mentioned above. While this is not an impediment for the design of the cryogenic control electronics where MOSFETs are biased in the saturation region at large V_{DS} [7], [11], it is crucial when the MOSFET is operated as a QD qubit and monolithically integrated with the control electronics, as proposed recently [7][8][10][12][13]. The latter idea is supported by the recent demonstration of silicon-based QD spin qubit operation above 1 K [14][15] where cryostats can more easily remove the heat dissipated by the control electronics, thus allowing for integration of more complex quantum processor units (QPUs) with thousands of qubits and associated control electronics on the same silicon die. For the design of such monolithic QPUs, a compact MOSFET model is required that is accurate down to their intended operating temperature. The model must feature not only temperature-dependent updates to the classical model parameters and equations to match the observed threshold voltage and subthreshold slope behaviour as in [2], but also quantum transport and Coulomb Blockade more commonly studied in the context of single electron/hole transistors, SETs/SHTs [16].

In this work we report a compact analytical model that captures the quantum phenomena present in MOSFETs at low temperature and demonstrate how it can be combined with a classical MOSFET design-kit model to reproduce measured nanoscale MOSFET behaviour in a circuit simulation environment. Section II describes the model equations and proposes a method to extract the model parameters directly from measurements. Section III compares the model to measurements of the minimum size p-MOSFET in a production fully-depleted silicon-on-insulator (FDSOI) CMOS process down to 6.2 K and showcases a circuit simulation example of the model. The significance of this work is discussed in Conclusions.

II. ANALYTICAL QUANTUM DOT MOSFET MODEL

A. Model Equations

The MOSFET drain-source current (I_{DS}) is modelled as the sum of the conventional design kit MOSFET current, with adjustments to account for cryogenic effects [2], and the quantum tunnelling current due to Coulomb Blockade (I_t) of the corresponding SET/SHT. The schematic of this model is depicted in Fig. 1 for the case of a p-MOSFET. To observe Coulomb Blockade, two conditions must be satisfied. First, the source and drain access resistances to the QD should each be larger than h/q^2 = 25.8 kΩ (where h is Planck's constant and q is the electron charge). Second, the energy required to add the ith electron/hole to the QD ($E_{add,i}$) must be larger than the thermal energy (k_bT where k_b is Boltzmann's constant) [17]. The latter condition is defined by

$$E_{add,i} = E_{C,i} + \Delta E_{i-1} = \frac{q^2}{C_{tot,i}} + \Delta E_{i-1} \gg k_bT \quad (1)$$

where

$$C_{tot,i} = C_{t,G,i} + C_{t,D,i} + C_{t,S,i} + C_{t,BG,i} \quad (2)$$

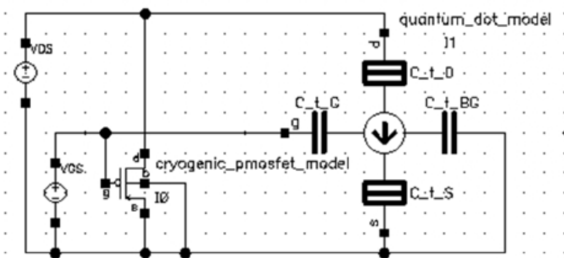

Fig. 1. Compact model schematic with foundry p-MOSFET (I0), adapted to fit classical cryogenic behaviour, in parallel with a single-hole transistor model implemented in verilog-A (I1). The subscript t is used to indicate circuit elements needed to model tunnelling and to disambiguate from traditional MOSFET parasitic capacitances.

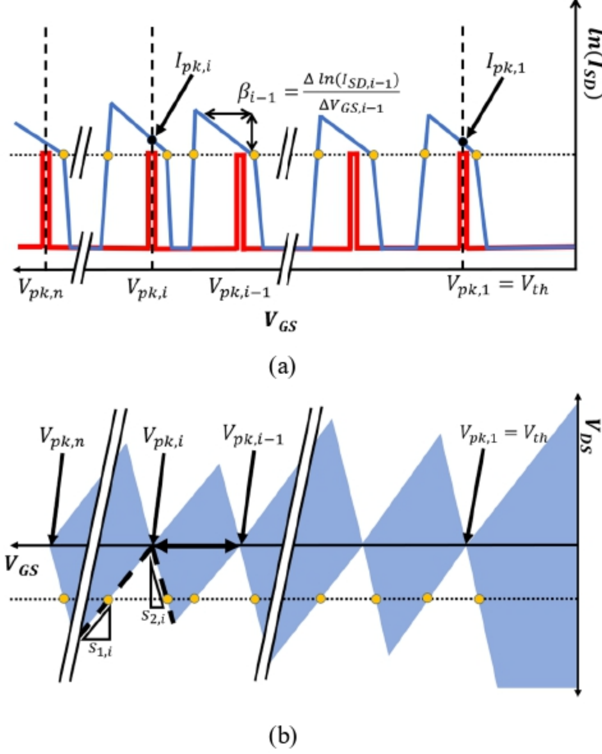

Fig. 2. Sample a) transfer characteristics with $ln(I_{SD})$ shown on y-axis vs V_{GS} biased at $|V_{DS}| = 20\,mV$ (blue) and $|V_{DS}| = 5\,mV$ (red) and b) corresponding stability diagram (i.e. $I_{DS}(V_{DS}, V_{GS})$) of a p-MOSFET operating as a single hole transistor. Blue shaded diamond areas represent valley regions in the drain current. Extraction of $I_{pk}, \beta, V_{pk}, s_1$ and s_2 is illustrated graphically along with V_{th} definition as the V_{GS} value associated with the first current peak.

and $E_{C,i} = q^2/C_{tot,i}$ is the charging energy required to overcome the Coulomb Blockade when adding the ith electron/hole to the QD. $C_{t,G,i}$, $C_{t,D,i}$, $C_{t,S,i}$ and $C_{t,BG,i}$ represent the intrinsic capacitances between the QD and the gate, drain, source and back-gate terminals of the MOSFET, respectively, while ΔE_i describes the eigenenergy spacing between the ith and next lowest eigenenergy solution of the QD [17]. Assuming that only the two most likely (i, i-1) electrons/holes in the QD contribute and that there are no co-tunnelling events [18], the expression of the tunnelling current at the ith peak (Fig. 2a) in the transfer characteristics (I_{DS}-V_{GS}) can be cast as

$$I_{t,i} = q_C \frac{T_S^+(i-1)T_D^-(i) - T_S^-(i)T_D^+(i-1)}{T_S^+(i-1)+T_S^-(i)+T_D^+(i-1)+T_D^-(i)} \quad (3)$$

where $q_C = \pm q$ for holes and electrons, respectively, and $T_S^{\pm}(i)$ represents the electron/hole tunnelling rate between the source and QD when the number of electrons/holes in the QD changes from i to $i \pm 1$. Similarly, $T_D^{\pm}(i)$ describes the corresponding tunnel rate between the drain and QD. Assuming a constant density of states in the source and the drain regions, tunnelling rates for QDs with large discrete energy level spacing ($\Delta E_i > k_b T$) are given by (4) – (8) [19] – [21].

$$T_{S/D}^{\pm}(i) = \frac{\Gamma_{S/D}(i)}{1+\exp\left(\frac{-\Delta F_{S/D}^{\pm}(i)}{k_b T}\right)} \quad (4)$$

$$\Delta F_S^-(i) = -\Delta F_S^+(i-1) = \frac{q_c}{C_{tot,i}}\left[C_{t,D,i}V_{DS} + \cdots \right.$$
$$\left. C_{t,G,i}\left(V_{GS} - V_{pk,i-1}\right) + Q(i)\right] + |\Delta E_{i-1}| \quad (5)$$

$$\Delta F_D^-(i) = -\Delta F_D^+(i-1) = \frac{q_c}{C_{tot,i}}\left[-\left(C_{tot,i} - C_{t,D,i}\right)V_{DS} + \cdots \right.$$
$$\left. C_{t,G,i}\left(V_{GS} - V_{pk,i-1}\right) + Q(i)\right] + |\Delta E_{i-1}| \quad (6)$$

$$V_{pk,i} = V_{th} - \sum_{j=2}^{i}\left[\frac{q_c}{C_{t,G,j}} + \frac{C_{tot,j}}{C_{t,G,j}}\left(\frac{\Delta E_{j-1}}{q_c}\right)\right] \quad (7)$$

$$\mathrm{Q(i)} = \begin{cases} 0 & i = 1 \\ q_C & i \neq 1 \end{cases} \quad (8)$$

where ΔF represents the change in the energy of the system and $\Gamma_{S/D}$ is the tunnelling rate coefficient of the indicated charge transfer event. The modified energy expressions in (5) and (6) account for the change with V_{GS} and V_{DS} in the QD capacitance, which is not captured by the orthodox Coulomb Blockade theory [17], while retaining a simple linear form. The analytical solution for $\Gamma_{S/D}$ requires knowledge of the energy barrier shape in the source and drain tunnel junctions, but its effect on I_{DS} can be approximated using a simple expression for the ith tunnelling current peak:

$$I_i(V_{GS}) = q\frac{\Gamma_D(i)\cdot\Gamma_S(i-1)}{\Gamma_D(i)+\Gamma_S(i-1)} = 2I_{pk,i}\exp\left[\beta_i\left(V_{GS} - V_{pk,i}\right)\right] \quad (9)$$

where $I_{pk,i}$ and β_i are parameters extracted from measurements. Substituting (4) through (9) into (3) and summing over all n tunnelling peaks (i.e. all n electrons/holes which can be stored in the QD) while satisfying (1), the expression of the total tunnelling current becomes

$$I_t = \sum_{i=1}^{n} \frac{I_i(Vgs)\cdot\left[1-\exp\left(\frac{q_C V_{DS}}{k_B T}\right)\right]}{\left[1+\exp\left(\frac{\Delta F_S^-(i)}{k_b T}\right)+\exp\left(\frac{-\Delta F_D^-(i)}{k_b T}\right)+\exp\left(\frac{q_C V_{DS}}{k_B T}\right)\right]} \quad (10)$$

B. Model Parameter Extraction

The complete list of model parameters for $I_t(V_{DS}, V_{GS})$ is V_{th}, $C_{tot,i}$, $C_{t,G,i}$, $C_{t,D,i}$, ΔE_i, $I_{pk,i}$, and β_i where the index i indicates that the parameter is used for modelling the ith current peak. Figs. 2a and 2b illustrate the idealized SHT behaviour observed in the I-V characteristics of a p-MOSFET QD and how these model fitting parameters can be defined and extracted from measured data. V_{th} is defined as the V_{GS} value at which the first tunnelling current peak occurs in the transfer characteristics measured at small $|V_{DS}| \approx 0\ V$. Next, for even i, the eigenenergy spacing is estimated assuming an infinite 1D rectangular potential profile with the well width given by the MOSFET gate finger width (W_f):

$$\Delta E_i \approx \begin{cases} 0 & i = odd \\ (i+1)\frac{h^2}{8m_{eff}W_f^2} & i = even \end{cases} \quad (11)$$

The odd i eigenenergy spacing is 0 to account for a spin degeneracy of 2. m_{eff} is the effective mass of the electron/hole along the width of the MOSFET. This approximation for ΔE_i is valid for the first few electrons/holes in FDSOI MOSFETs where an effectively infinite potential barrier, due to the top and bottom gate oxides, and due to shallow trench isolation oxides, surrounds the channel in two

dimensions [7]. $I_{pk,i}$ are obtained from the measured transfer characteristics in the triode region at relatively large $|V_{DS}|$ ($\geq 6k_bT/q$), blue curve in Fig. 2a. In this work, $|V_{DS}| = 20$ mV was used. $V_{pk,i}$ represent values of V_{GS} corresponding to the the ith tunnelling peak obtained from a transfer characteristic measured at small V_{DS}, red curve in Fig. 2a. In this work $|V_{DS}| = 5$ mV was used. Parameters β_i are estimated from the slope of the ith peak of the transfer characteristic at $|V_{DS}| = 20\ mV$ (blue curve in Fig. 2a) when plotted on a logarithmic scale. The capacitance parameters are extracted using (12) – (14) from the estimated slopes $s_{1,i}$ and $s_{2,i}$ defined by the dashed lines in the stability diagram, Fig. 2b. These lines, of constant current, demarcate the Coulomb Blockade regions.

$$C_{t,G,i} = \left| \frac{q_C}{(V_{pk,i} - V_{pk,i-1}) - \left(\frac{s_{2,i} - s_{1,i}}{s_{1,i}s_{2,i}}\right)\left(\frac{\Delta E_{i-1}}{q_C}\right)} \right| \tag{12}$$

$$C_{t,D,i} = \left| \frac{C_{t,G,i}}{s_{2,i}} \right| \tag{13}$$

$$C_{tot,i} = C_{t,G,i} \left| \frac{s_{2,i} - s_{1,i}}{s_{1,i}s_{2,i}} \right| \tag{14}$$

Since there is no $V_{pk,0}$ ($V_{pk,1} = V_{th}$ is the first peak location), (12) cannot be used to find $C_{t,G,1}$. Instead, the $C_{t,G,1} \approx C_{t,G,2}$ approximation is applied. Similarly, one of the slopes s_1 or s_2 will be masked at the n^{th}(last) peak by the classical MOSFET current. Therefore, to extract the capacitances, it is assumed that $s_{1/2,n} \approx s_{1/2,n-1}$.

III. Results Discussion

A single-finger FDSOI p-MOSFET with gate length $L_G = 18$ nm and finger width $W_f = 70$ nm was fabricated in a production 22nm FDSOI CMOS process [22] for characterization and model validation. Measurements were conducted in a closed-cycle cryostat from 6 – 300 K using a Keithley 4200A-SCS parameter analyzer with ~1s integration times to reduce the current measurement noise floor to ~100fA (limited by the setup). Model parameters were extracted from measurements, Fig. 3, in the QD bias regime (i.e. subthreshold triode region) at 6.2 K and are tabulated in Table 1. Using these parameters and (5) - (11), the I-V characteristics of the device were reproduced in Fig. 4 and Fig. 5. An effective hole mass $m_{eff} = 0.08\ m_0$ was assumed for computing ΔE_i, consistent with that published in the literature for compressively strained $Si_{0.75}Ge_{0.25}$ [23]. The same model parameters extracted at 6.2 K were used up to 50 K to compare model accuracy to measurements over temperature. The comparison of the measured and modelled transfer characteristics in Fig. 5 demonstrates that model extraction at 6.2 K can be used to reproduce the characteristics at up to 50K.

Fig. 6 shows the simulated p-MOSFET transfer characteristics from 1 K to 300 K to demonstrate its seamless use over a wide range of temperatures. Finally, Fig. 7, illustrates the application of the model to simulate the transfer characteristics at 2 K of a p-type QD integrated with the 104 dBΩ transimpedance amplifier in the same test setup used for the measurements reported in [11]. This is an example of a qubit readout circuit based on SHT current amplification from a few nA to a few mV directly into a 50 Ω load with higher bandwidth than would be achievable with the small p-MOSFET driving the load directly.

IV. Conclusion

Cryogenic measurements of the minimum size p-MOSFET fabricated in a production FDSOI CMOS process were used to demonstrate a compact DC I-V characteristic model which adds a tunnelling component on top of the classical MOSFET foundry model to capture quantum and Coulomb Blockade effects. A methodology was developed to extract the model parameters from a single set of DC I-V characteristics measured at 6 K. Since it includes the classical design kit MOSFET model, the proposed QD model can be used to seamlessly reproduce DC I-V characteristics and high frequency performance from 1 K to 400 K with reasonable accuracy below 70 K and with the same accuracy as the design kit model in the normal range of temperatures used in IC design. This work represents a significant step towards the development of a complete simulation environment for the design of QPUs in which semiconductor quantum dot qubits are monolithically integrated with their control/readout electronics.

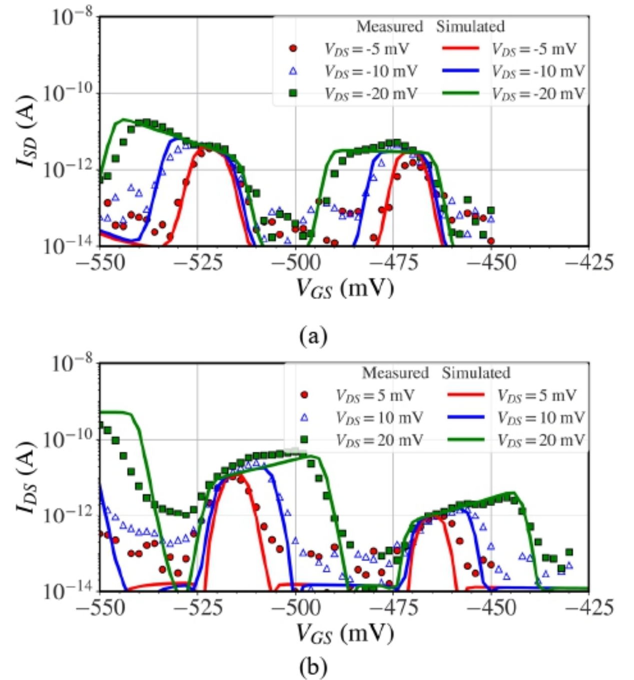

Fig. 3. Measured (symbols) vs simulated (lines) 6.2K transfer characteristics biased at different a) negative and b) positive V_{DS}.

Table 1. Extracted QD model parameters for 18nmx70nm p-MOSFET

Peak No.	Model Parameter*				
	$C_{tot,i}$ (aF)	$C_{t,G,i}$ (aF)	$C_{t,D,i}$ (aF)	$I_{pk,i}$ (pA)	β_i (V^{-1})
1	4.3 / 4.8	3.2	0.6 / 0.6	2.9 / 0.85	5.2 / -70
2	5.12 / 4.8	3.2	0.7 / 0.7	3.7 / 11	80 / -56
3	7 / 5.6	3.7	0.8 / 0.8	0.33 / 475	100 / 0
V_{th} = -468 mV			$m_{eff} = 0.08m_0$		

* Values indicated for negative/positive V_{DS}.

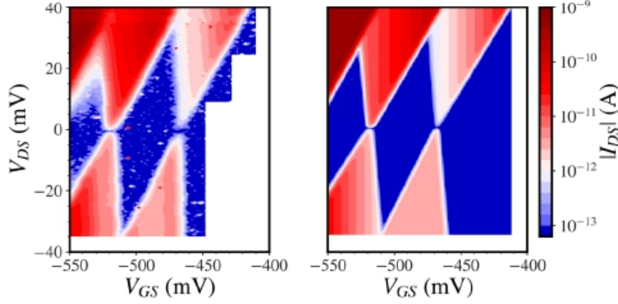

Fig. 4. Measured (left) vs simulated (right) stability diagram (i.e. $I_{DS}(V_{DS}, V_{GS})$) for 1x18nmx70nm p-MOSFET at 6.2 K.

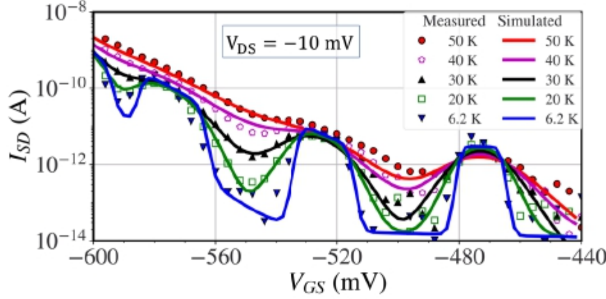

Fig. 5. Measured (symbols) vs simulated (lines) transfer characteristics for V_{DS} = -10 mV at different temperatures.

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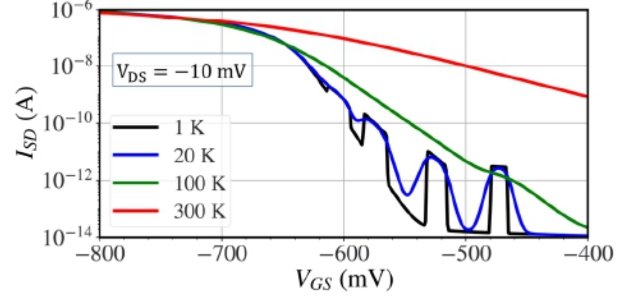

Fig. 6. Simulated transfer characteristics at V_{DS} = -10 mV and T = 1 K, 20 K, 100 K and 300 K.

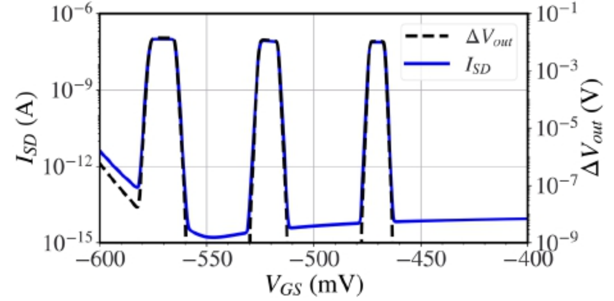

Fig. 7. Simulated transfer characteristics of a p-type SHT at 2 K and V_{DS} = -5 mV amplified by a cryogenic TIA co-integrated on-chip [11].

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