Towards Monolithic Quantum Processors in Production FDSOI CMOS Technology

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Outline

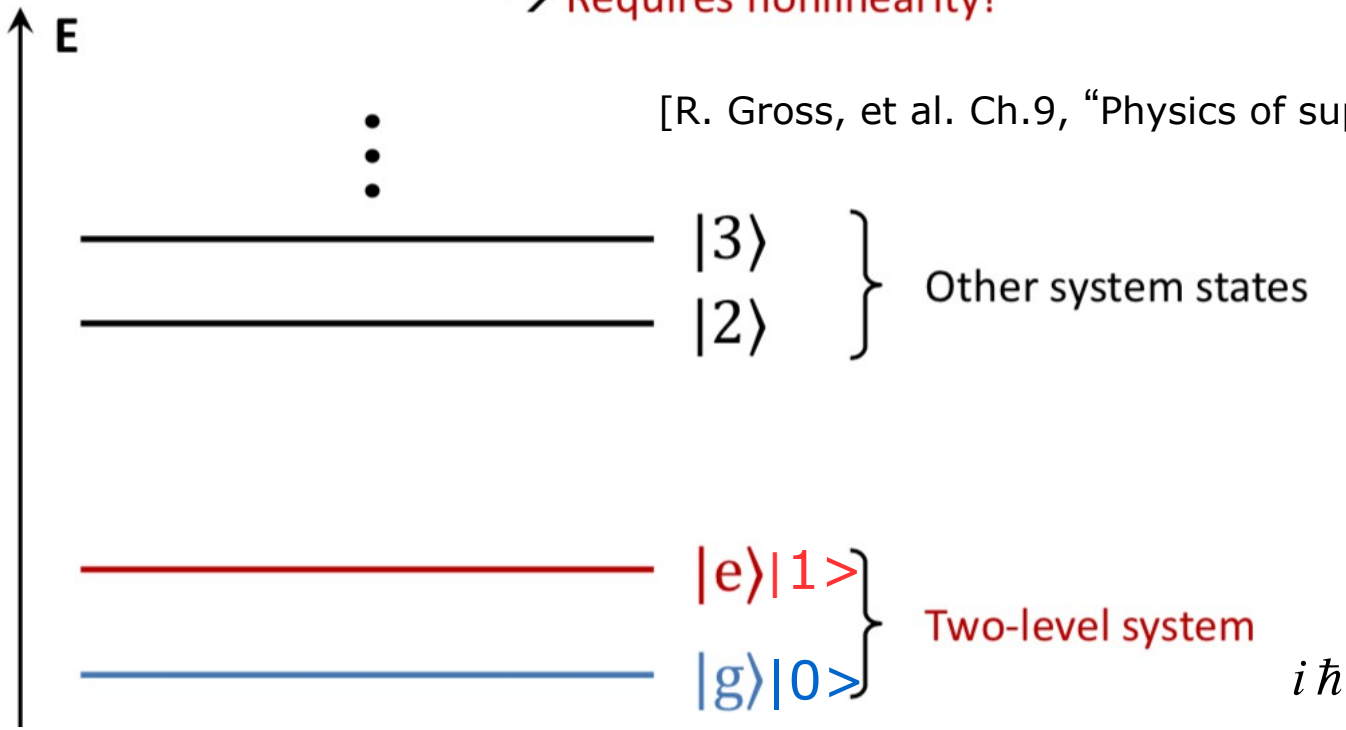
- **Introduction**
- Quantum Processor SoCs
- Cryogenic characterization of 22nm FDSOI CMOS Technology
- Conclusions

Two-level quantum system

Natural systems: → Natural spins $|\downarrow\rangle$, $|\uparrow\rangle$
→ Orthogonally polarized light $|\updownarrow\rangle$, $|\leftrightarrow\rangle$

Effective systems: → Isolate two levels from a manifold structure
Mechanisms: Energy separation, selection rules, …
→ Requires nonlinearity!

[R. Gross, et al. Ch.9, "Physics of superconducting quantum circuits," 2001-2018]

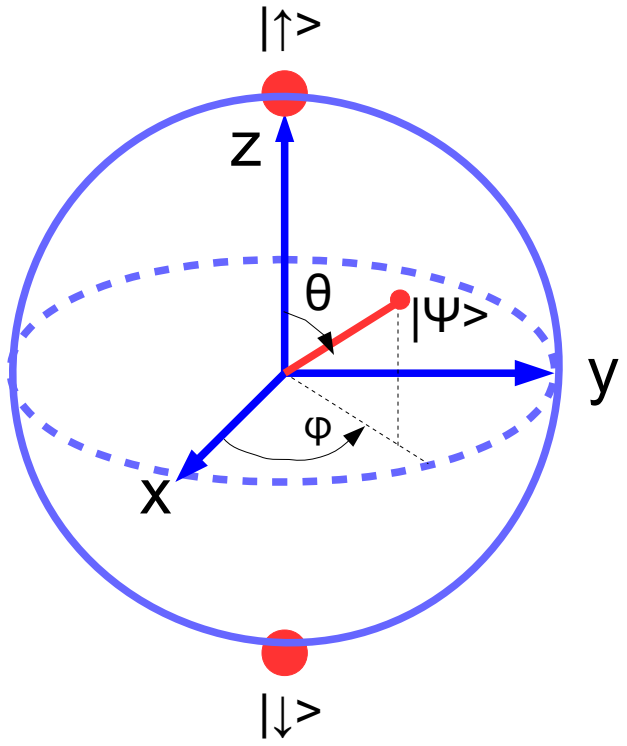


$$i\hbar\frac{d|\psi(t)>}{dt}=\hat{H}(t)|\psi(t)>=E(t)|\psi(t)>$$

Control of two-lvel system

- Qubit is pseudo spin
  - Independent of qubit realization
  - Methods from nuclear magnetic resonance
- Basic idea
  - **Coherently** rotate spins by static or oscillating magnetic fields
  - Static fields parallel to quantization axis => free precession, changes φ on Bloch sphere
  - Oscillating fields perpendicular to quantization axis => change population, changes θ on Bloch sphere

Bloch sphere



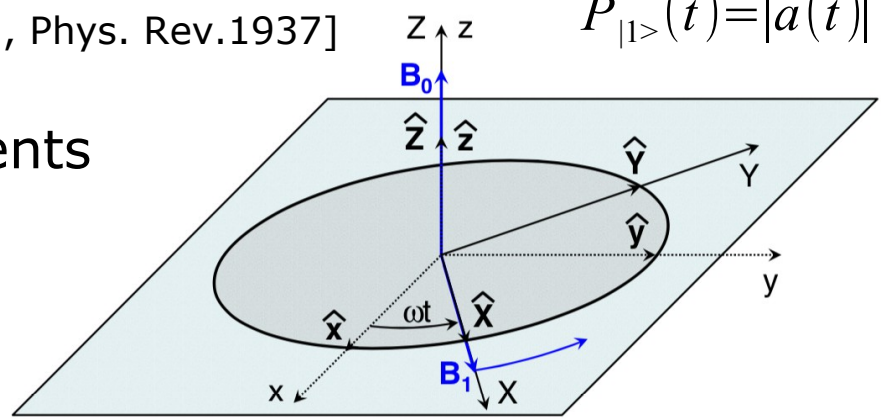
Spin ½ hamiltonian in a rotating magnetic field

$$\hat{H}_S = \frac{g\mu_B}{2}\hat{\sigma}\cdot\vec{B} = \frac{g\mu_B}{2}\begin{bmatrix} B_z & B_x - iB_y \\ B_x + iB_y & -B_z \end{bmatrix} \qquad i\hbar\frac{d}{dt}\mathrm{X}(t) = \frac{g}{2}\mu_B\begin{bmatrix} B_z & B_x - iB_y \\ B_x + iB_y & -B_z \end{bmatrix}\mathrm{X}(t) \qquad \mathrm{X}(t) = \begin{bmatrix} a(t) \\ b(t) \end{bmatrix}$$

$$\vec{B}(t) = B_{dc} + B_1(t) = (B_1\cos\omega t, B_1\sin\omega t, B_0)$$

[I.I. Rabi, Phys. Rev.1937]

$$P_{|1>}(t) = |a(t)|^2$$



***B*$_1$**(t) = rotating ac field, with quadrature components along **x,y** axes and with $B_1 << B_{dc}=B_0$

$$\omega_0 = \omega_L \stackrel{\text{def}}{=} \frac{g}{2}\frac{\mu_B}{\hbar}B_{dc} \qquad \omega_R \stackrel{\text{def}}{=} \frac{g}{2}\frac{\mu_B}{\hbar}B_1 \ll \omega_0$$

ω_0= qubit (Larmor) frequency, ω_R= Rabi frequency

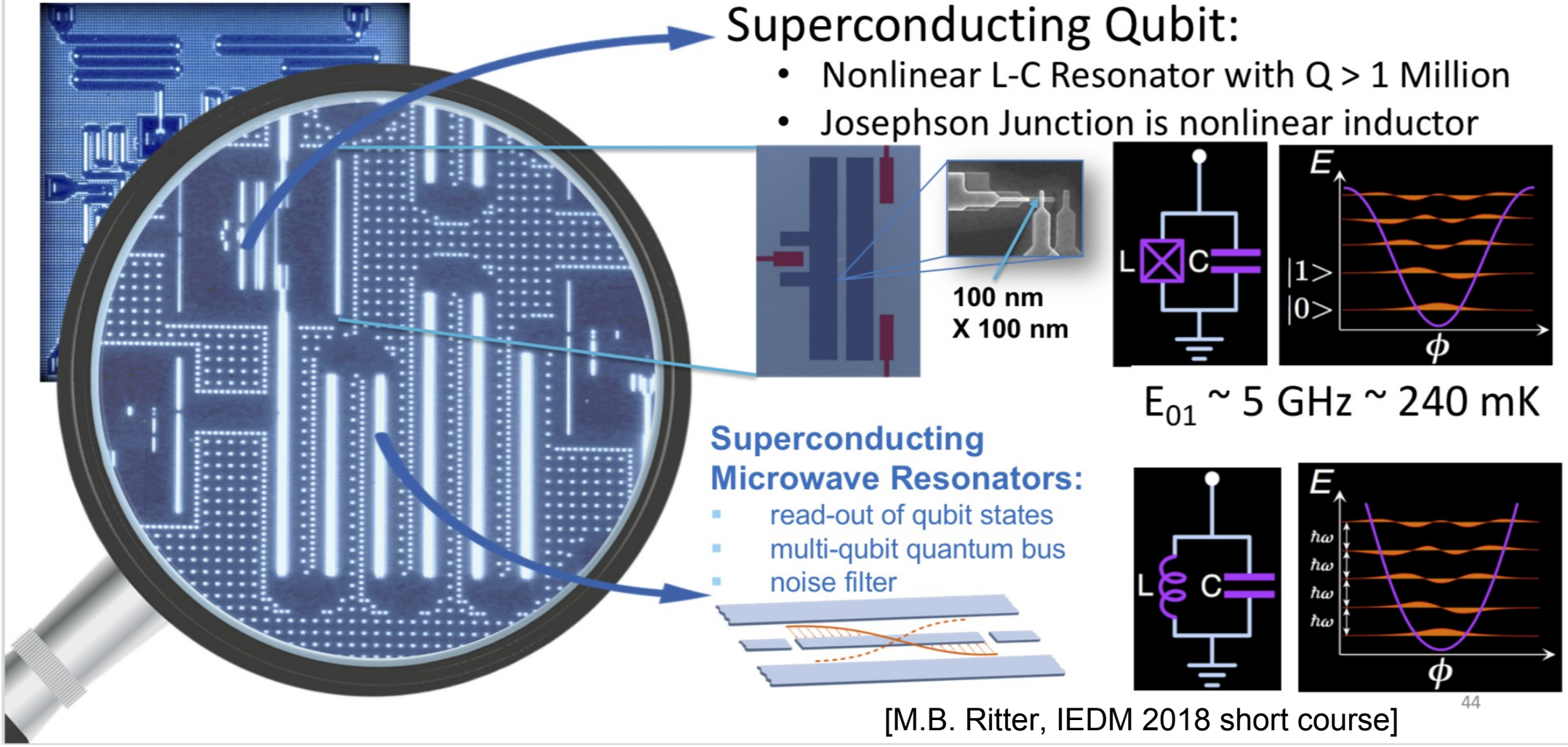
[R. Gross, et al. Appendix 10," 2001-2018]

$$\hat{H} = \frac{g}{2}\mu_B\begin{bmatrix} B_0 & B_1 e^{-j\omega t} \\ B_1 e^{j\omega t} & -B_0 \end{bmatrix} = \frac{\hbar}{2}\begin{bmatrix} \omega_0 & \omega_R e^{-j\omega t} \\ \omega_R e^{j\omega t} & -\omega_0 \end{bmatrix}$$

$\theta(t) = \theta =$ constant in time. $\phi(t) = \phi + \omega_0 t$

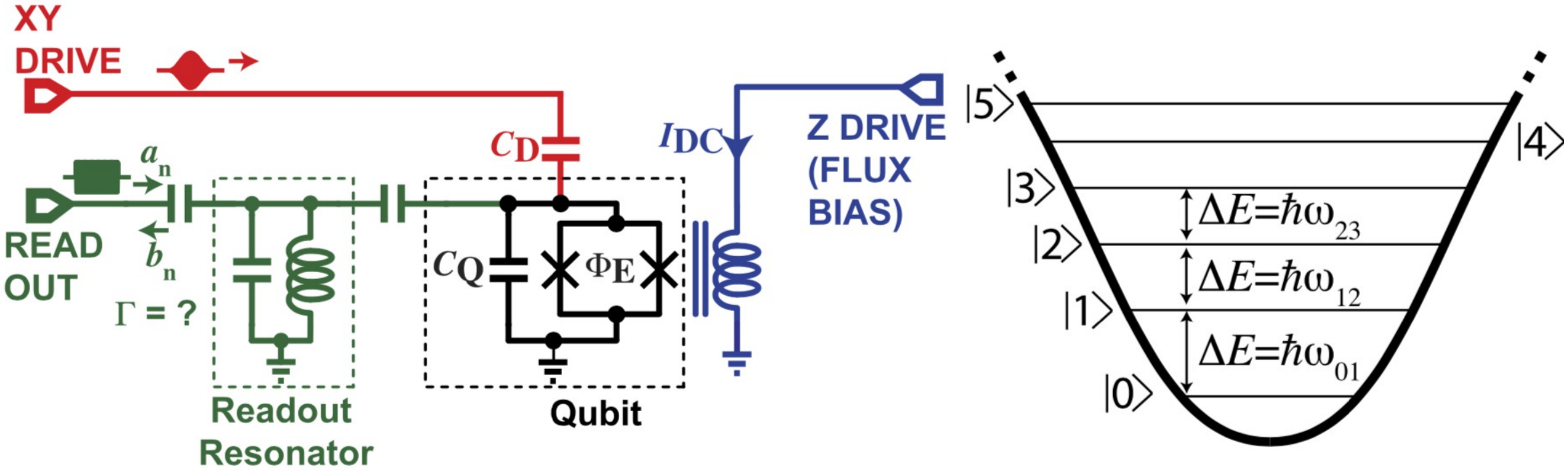
$U = e^{-i\hat{H}t}$ describes spin evolution in time $|\Psi(t)> = \cos\frac{\theta}{2}e^{-i(\psi+\omega_0 t)/2}|\uparrow> + \sin\frac{\theta}{2}e^{i(\psi+\omega_0 t)/2}|\downarrow>$

Superconducting qubits: most common today



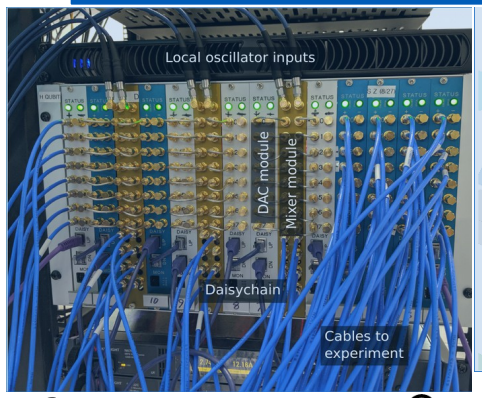
[M.B. Ritter, IEDM 2018 short course]

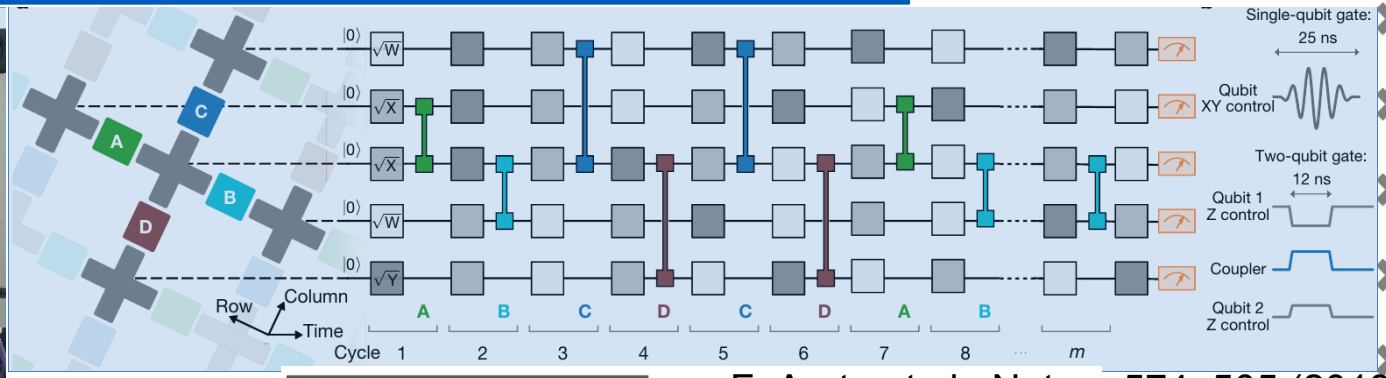
Google's Josephson junction transmon qubit

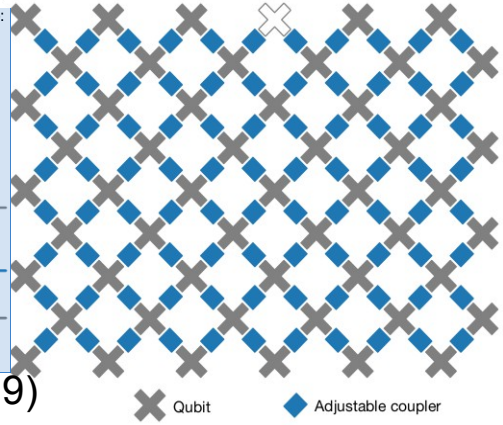


J. Bardin et al., JSSC, Nov. 2019

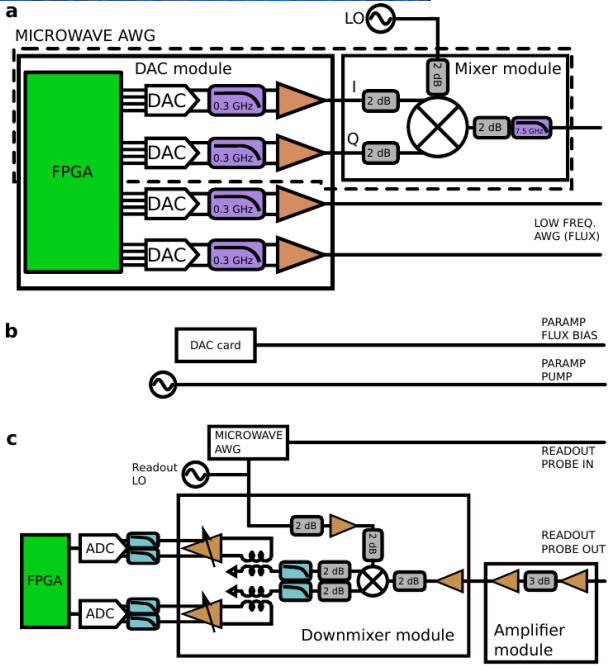
Google’s 54-qubit superconducting processor: 10 mK

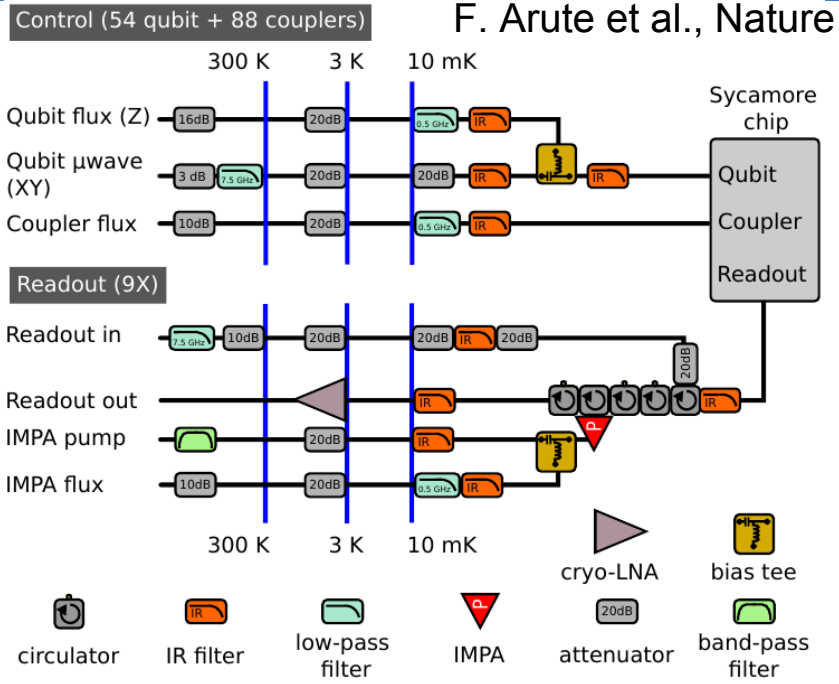


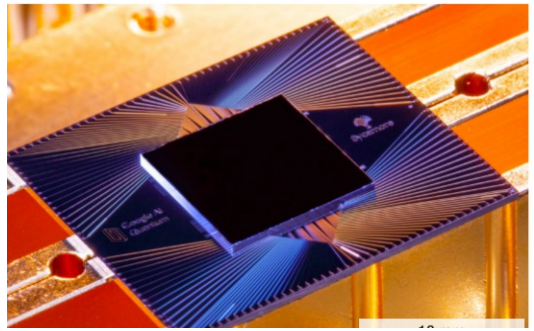


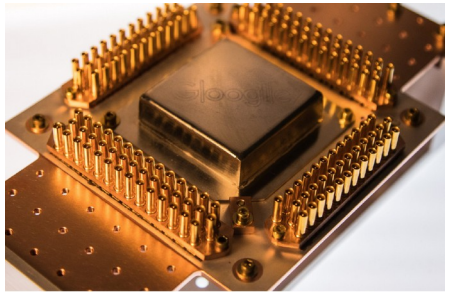


F. Arute et al., Nature 574, 505 (2019)

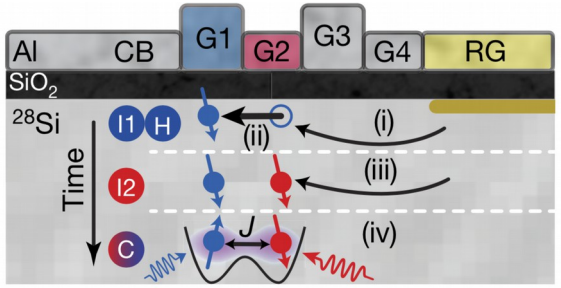




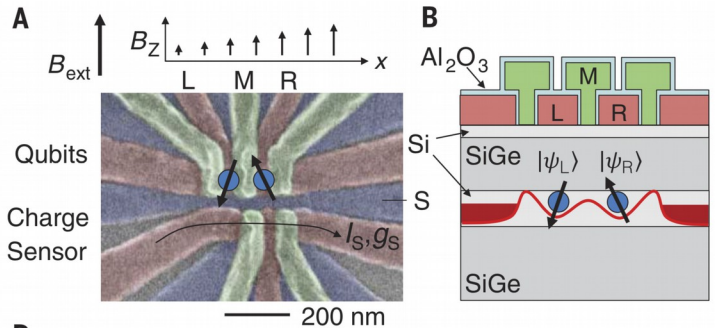




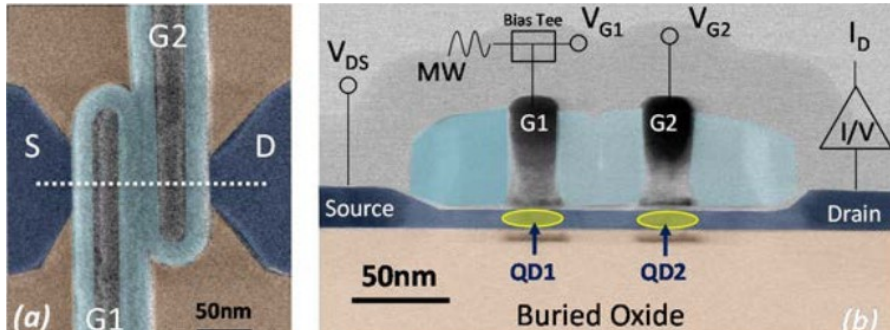
Semiconductor quantum dot qubits



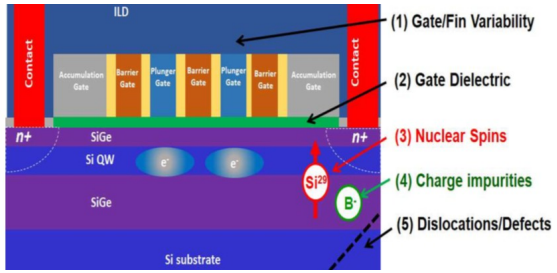
[W.Huang, Nature 2019]

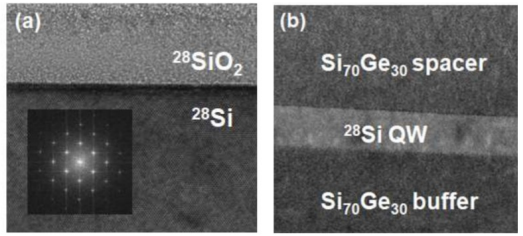


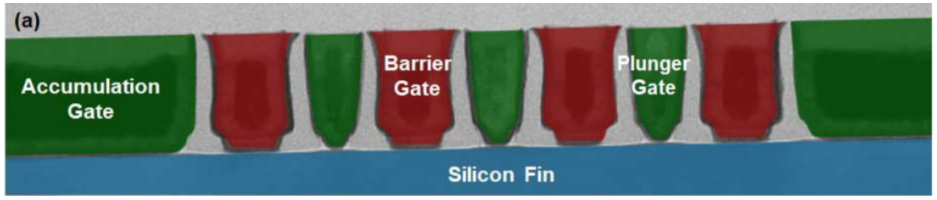
[D.M. Zajec, Science 2018]



[L. Hutin, VLSI 2016]







[Intel, IEDM 2018]

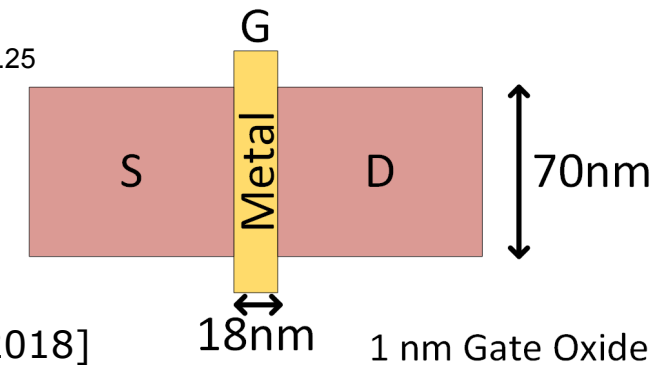
- Qubits formed in QDs where electrons/holes are confined by an energy potential well created in the conduction/valence band of a semiconductor structure: Si, Si/SiGe MOSFET, FDSOI, FinFET
- QDs placed in close proximity to enable coupling which is a function of barrier height/thickness
- Two adjacent (usually lowest) energy levels in QD used to create basis states |0> and |1>

Our approach and goals

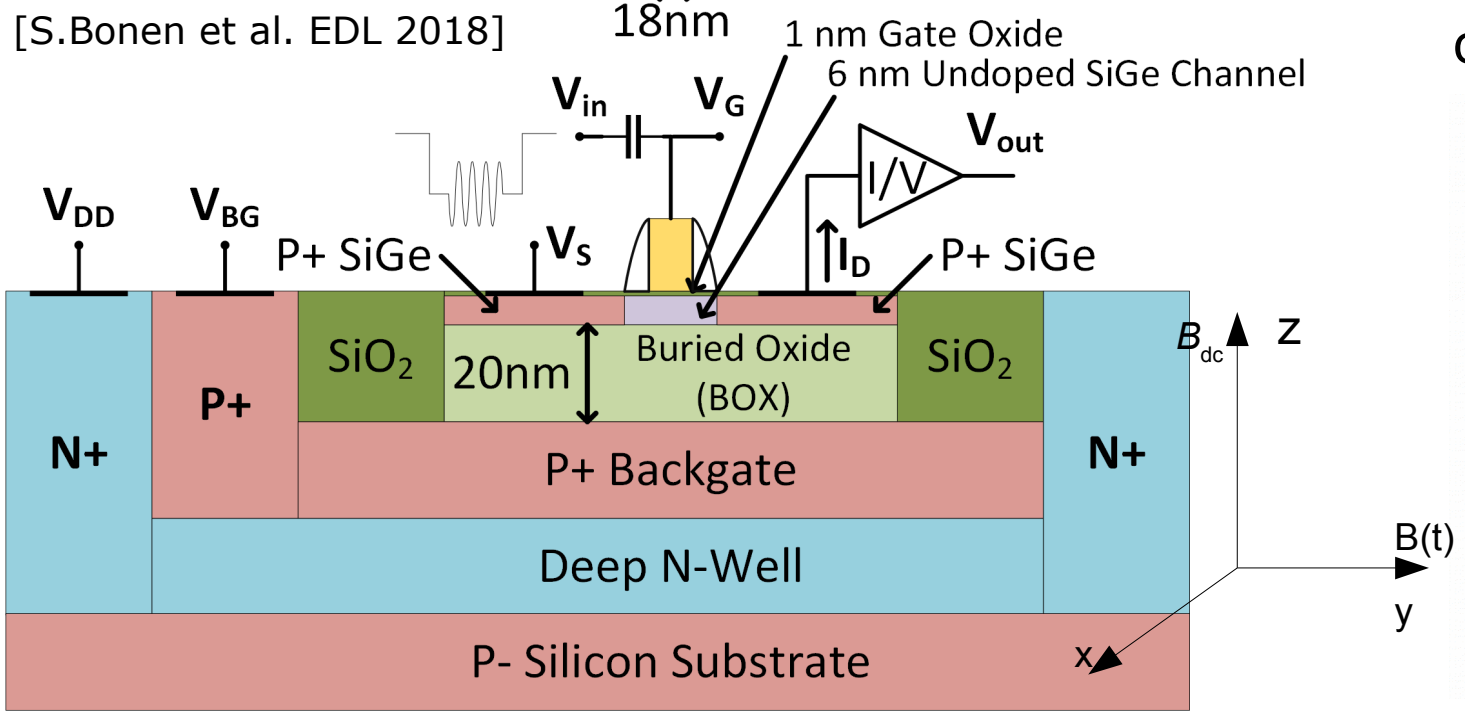
- ***Foundry FDSOI*** CMOS-based QD qubits
  - **SiGe p-MOSFET** with channel/S-D heterojunction for hole spin qubit
- Investigate same and new spin control and readout techniques as SC qubits
- ***mm-wave AMS circuits*** for spin manipulation and readout ***on the same die with the qubits***
- **2-4 *K*** operation now, ***(maybe) 77 K*** in 15 years

The SiGe p-MOSFET is the SiGe hole-spin qubit

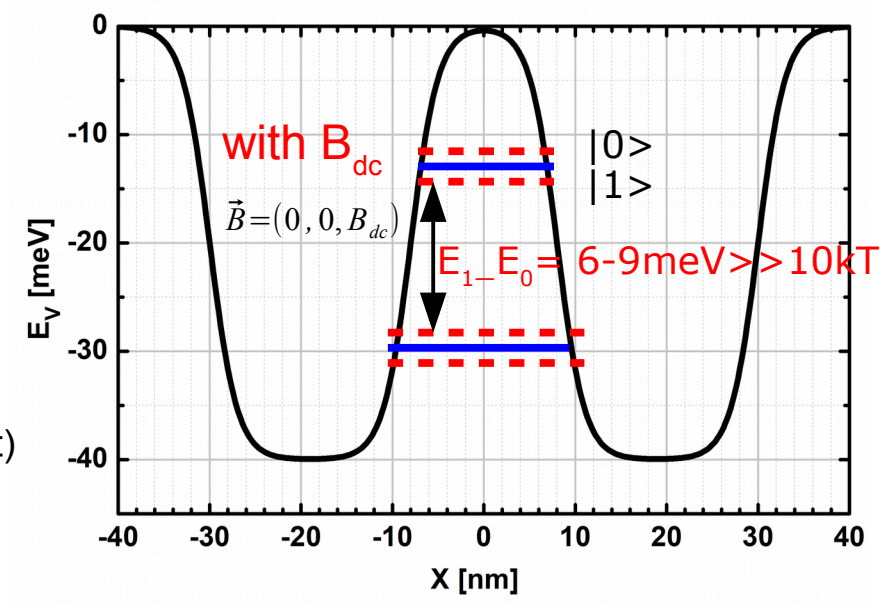
$Si_{0.7}Ge_{0.3}/Si_{0.75}Ge_{0.25}$



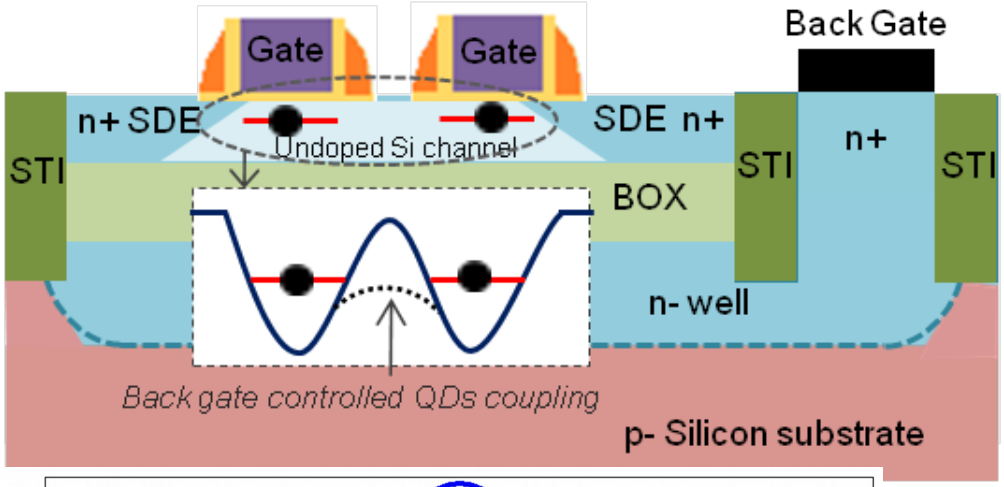
[S.Bonen et al. EDL 2018]

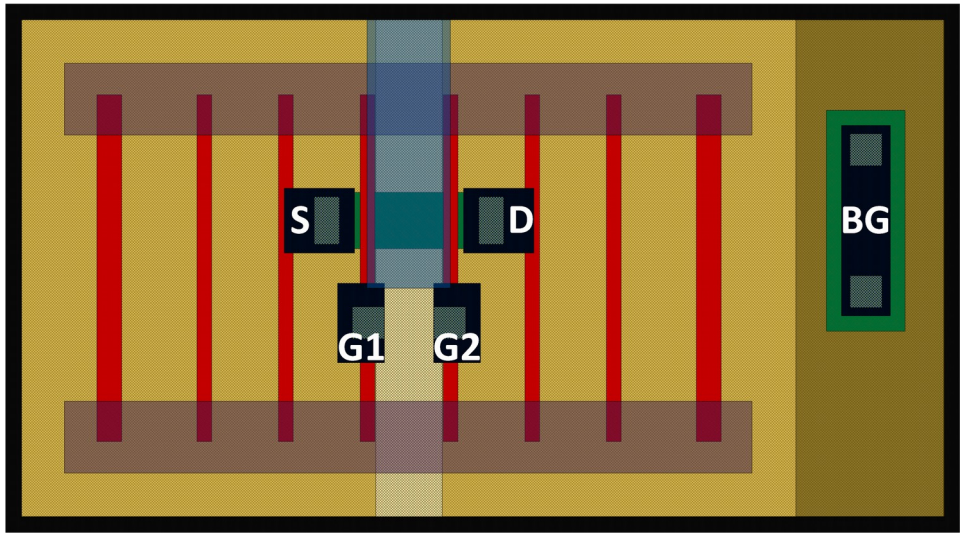


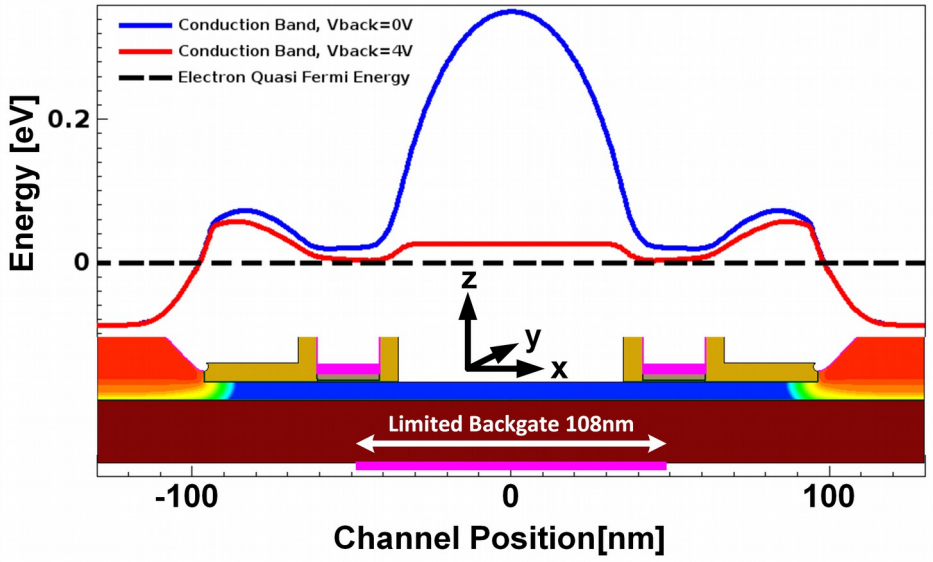
- L=18 nm; W = 50 nm
- source/drain-to-channel heterojunction: ΔE_V = 35-40 meV
- t_{oxe}= 1 nm => larger f_R than thick oxide/semiconductor qubits



Electron- and hole-spin DQD concept in FDSOI





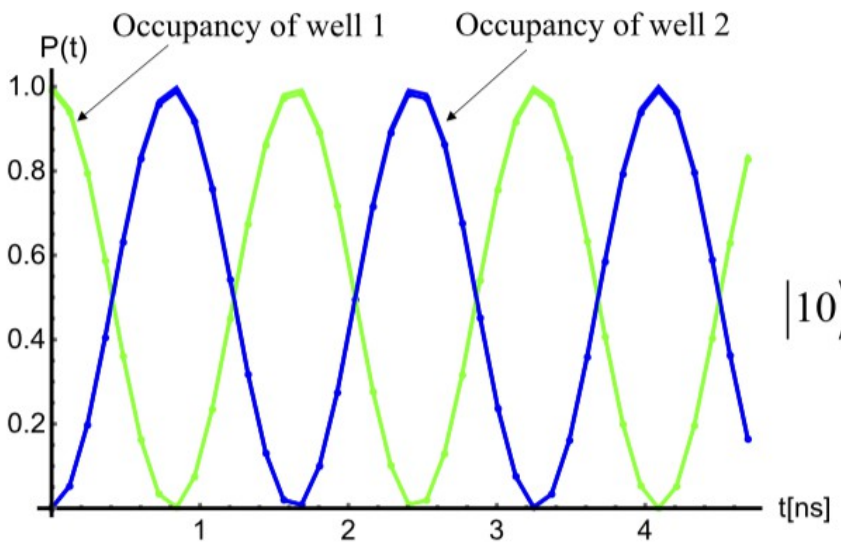


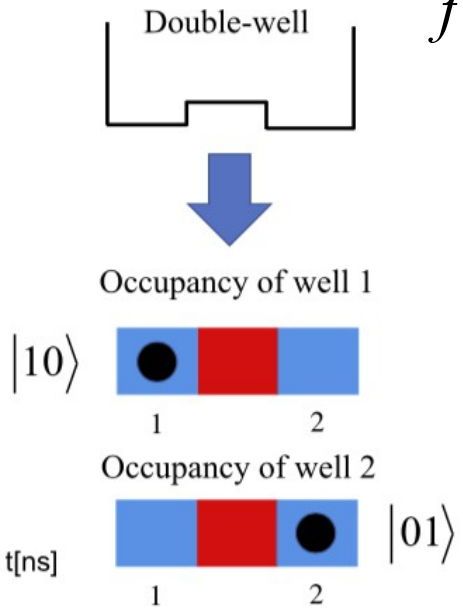
- Double quantum-dot (DQD) qubit = 2-gate MOSFET cascode
- Quantum dot (QD) under each top gate
- Individual gate control of each QD
- Potential barrier between dots
- Back gate for entanglement control **(needs special mask)**
- mm-wave E-field applied on gate and *z*-axis dc magnetic field

Charge qubit concept in FDSOI

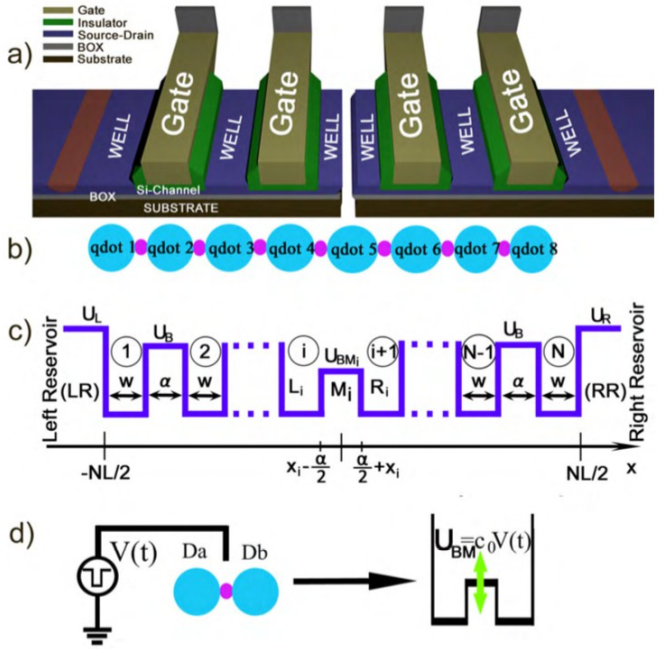
- Similar to charge coupled devices
- Gates control barriers (tunnel coupling, ***t***) between QDs
- Degree of freedom is position of electron in DQD
- Voltage applied between dots creates detuning: $E_{P1} \neq E_{P2}$
- Rabi frequency from probability oscillation

$$f_R = \frac{2t}{2\pi\hbar}$$





[P. Giounanlis et al. IEEE Access 2019]



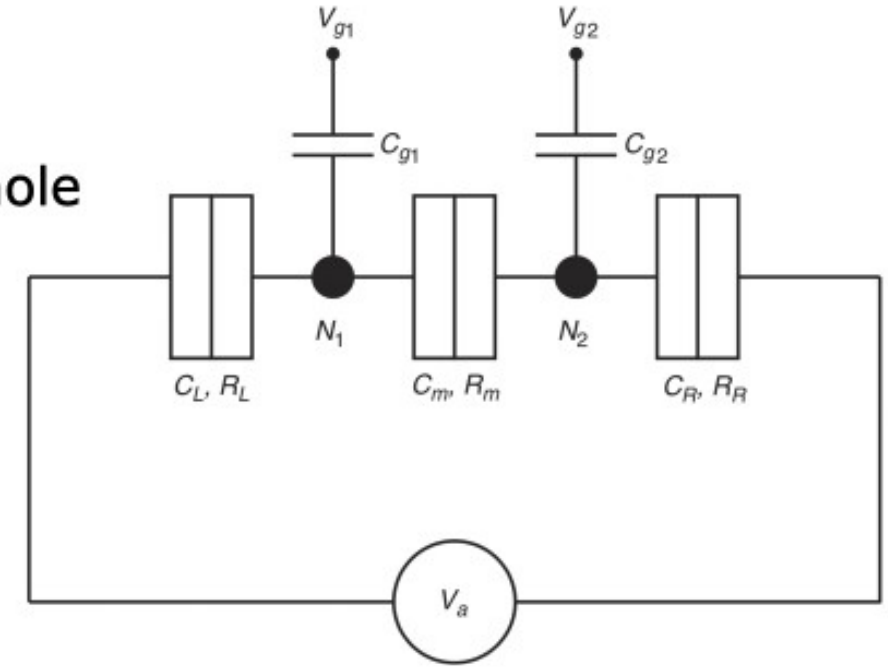
$$\hat{H} = \begin{bmatrix} E_{P1} & t \\ t & E_{P2} \end{bmatrix}$$

$$|\psi(t)> = a(t)|10> + b(t)|01>$$

Equivalent circuit of Double Quantum Dot

- Tunnel barriers described by R_t, C_t
- Gate-to-dot (channel) capacitance C_g = 20 aF ... 30 aF
- Use charge conservation analysis: $\Delta Q = C \times \Delta V_g$ as in switched capacitor circuits

  where $Q_{1,2} = N_{1,2} \times q$
- $q = 1.6 \times 10^{-19}$ C => ΔV_g = 3-5 mV per electron/**hole**



[D.K. Ferry, et al. Ch.6, Nanostructures, 2005]

Comparison to other qubit families

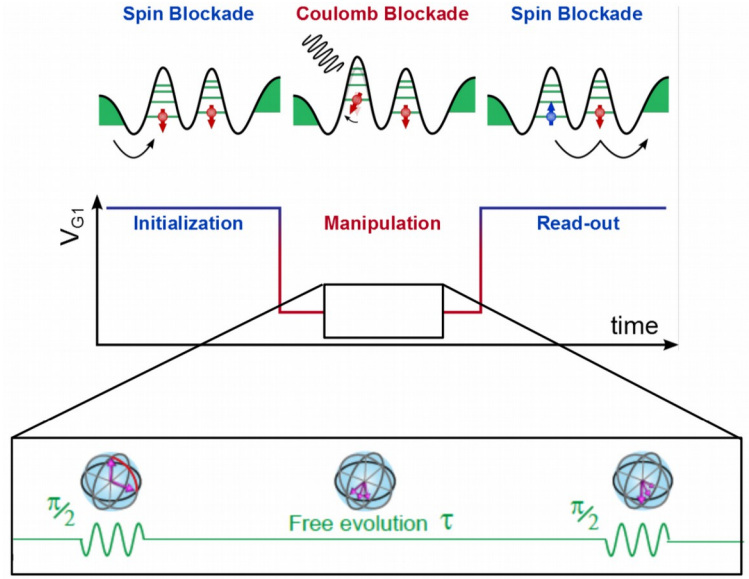
- >20x f_L, f_R compared to SC qubits:
  - > 20^2x smaller readout resonators, > 20x higher operation temp.
- Larger $\boldsymbol{g}$, f_R than vertically stacked SiGe/Si/SiGe FinFET qubit
- Backgate control for circuit V_T adjustment at low temperature
- Potential selective fast backgate for CNOT gate
- All spin control/readout schemes from SC qubits can be used

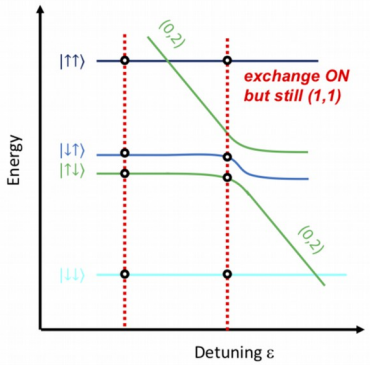
Outline

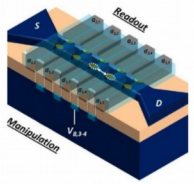
- Introduction
- **Quantum Processor SoCs**
- Cryogenic characterization of 22nm FDSOI CMOS Technology
- Conclusions

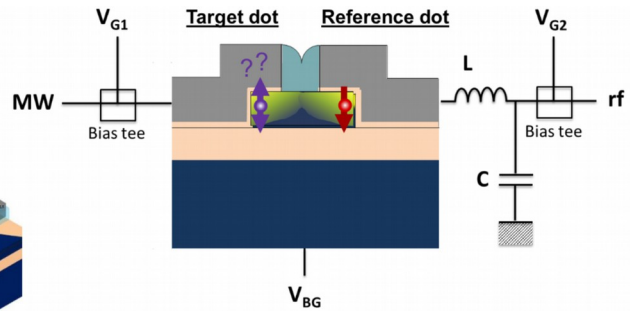
Classical controller

- **Three functions**
  - Initialization
  - Manipulation
  - Read-out
- **Phenomena employed**
  - Coulomb blockade
  - Pauli spin blockade
  - Quantum capacitance reflectometry









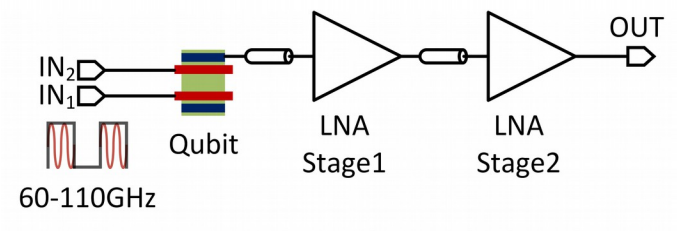
$$C_Q \propto \frac{\partial^2 E}{\partial^2 \varepsilon}$$

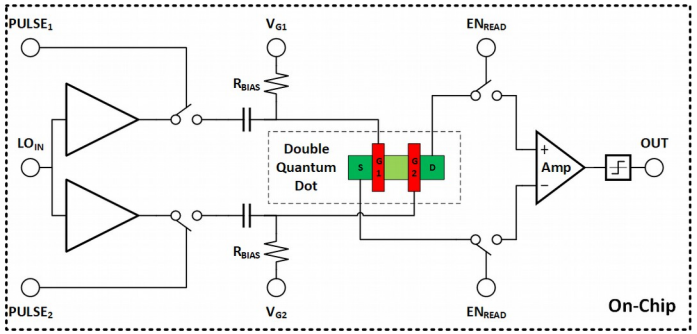
No RF_{out} shift
target qubit is ↓

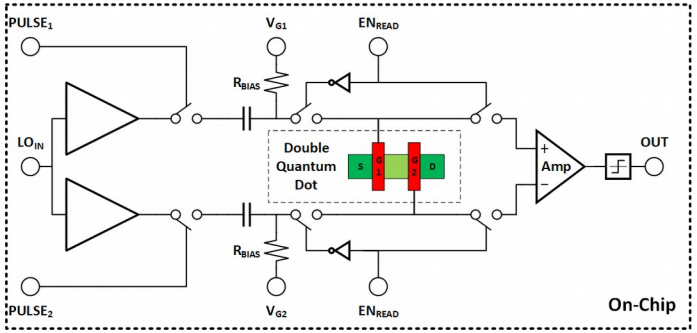
RF_{out} shift
target qubit is ↑

[L. Hutin, IMS 2019]

Readout schemes



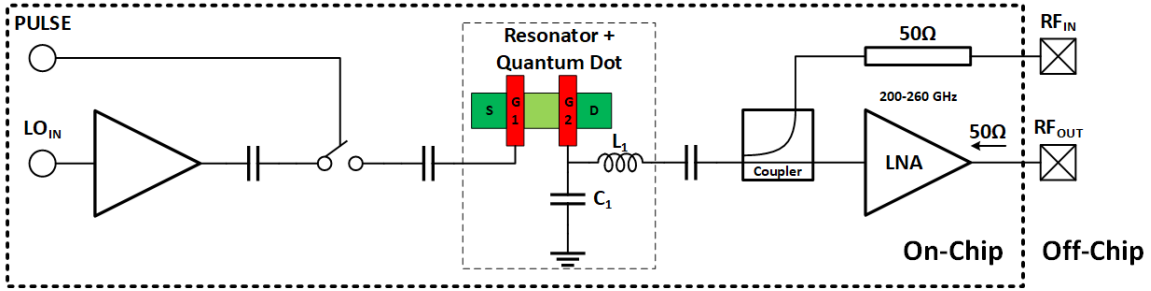




Nondemolition, dispersive (non-resonant)

- mm-wave reflection meas. (phase, amp)
  - narrow band
  - needs inductors (large area)
  - needs precision ADC

- Charge, current or voltage amplifier
  - SET/capacitive coupling needed
  - Broadband
  - Noisy, 1/f noise sensitive

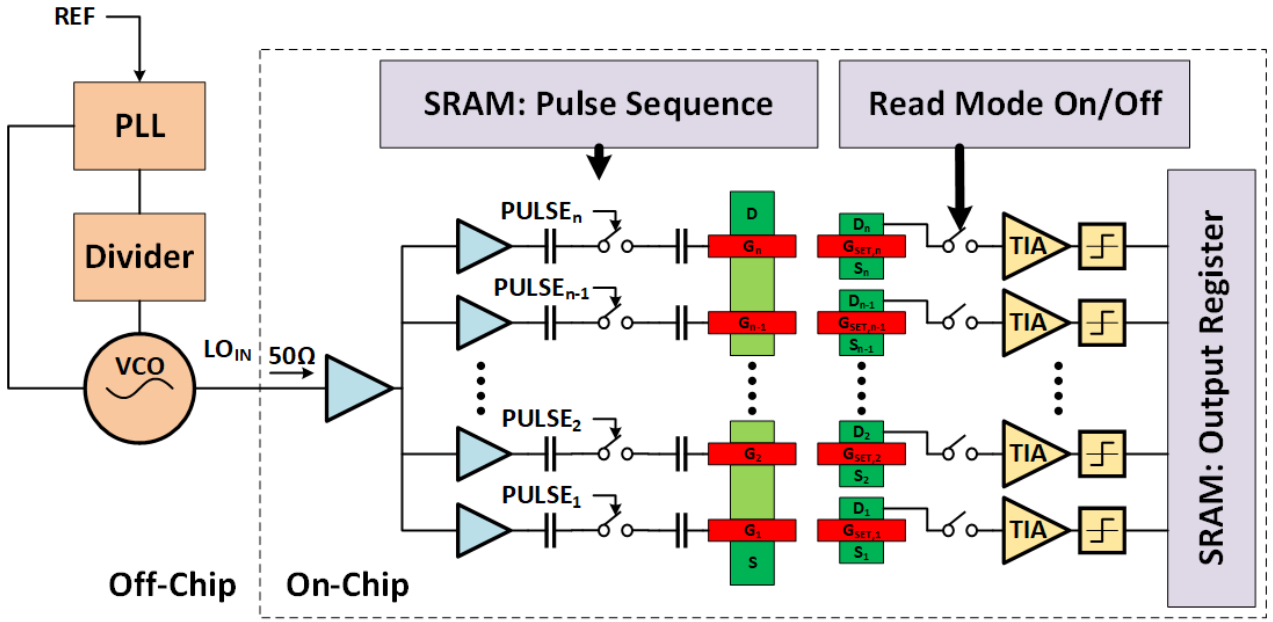


Hole-spin monolithic quantum processor

- **Qubit array**
  - 0.5 pW (10pA/50mV) per qubit
  - 10^{10} qubits = 5 mW
- **Spin manipulation**
  - low phase noise (OFDM) signal at f_L
  - 60-100 GHz for 3-5 K operation
  - 140-240 GHz for 8-12 K operation
  - n-MOSFET switch+phase pulse modulators

$$P_{dc}=0; \quad P=\frac{f_R}{2}C\cdot V_{DD}^{2}$$

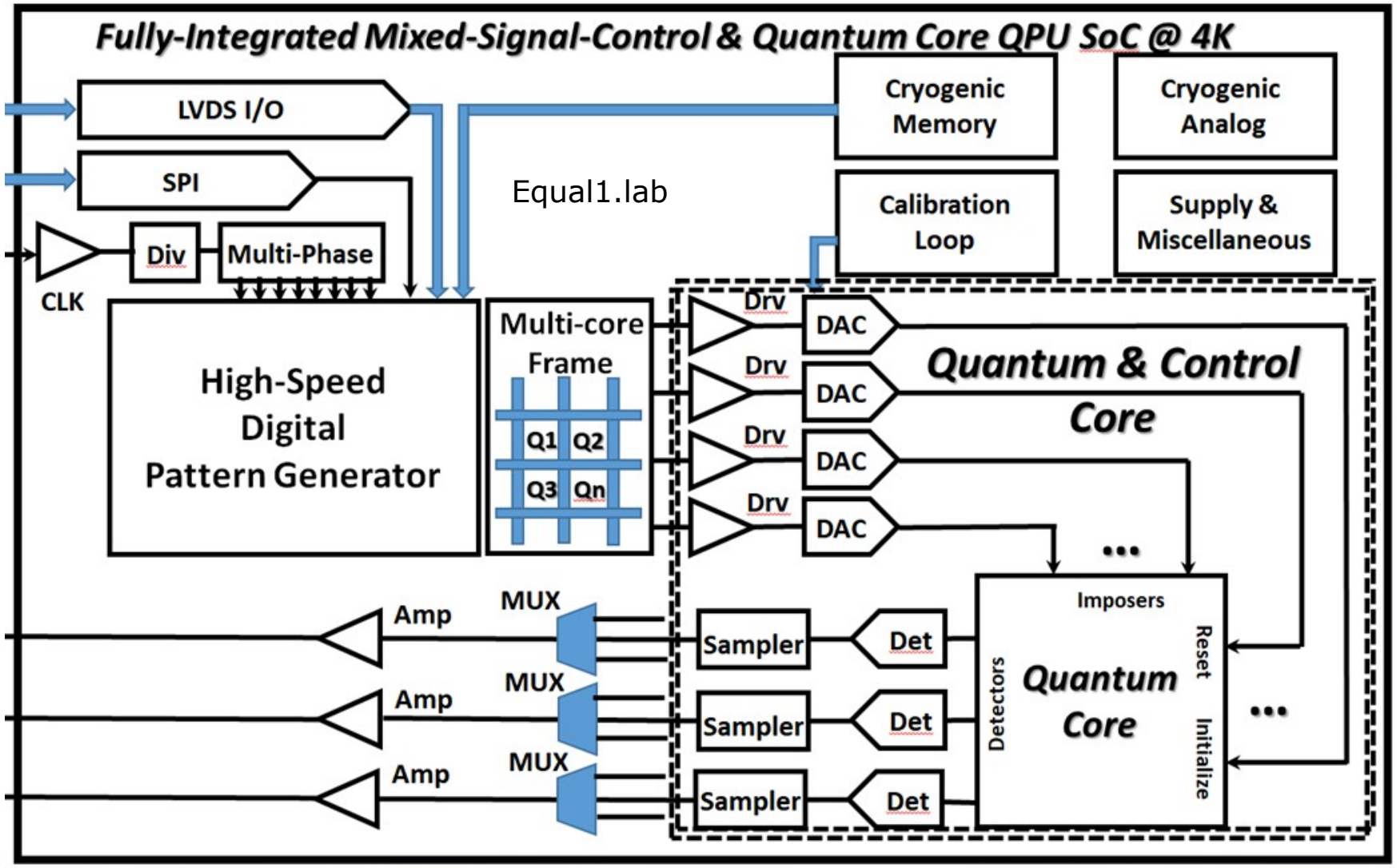
- **SRAM** stores digital pulse sequences (gate operations)



Note: qubit bias scheme not shown

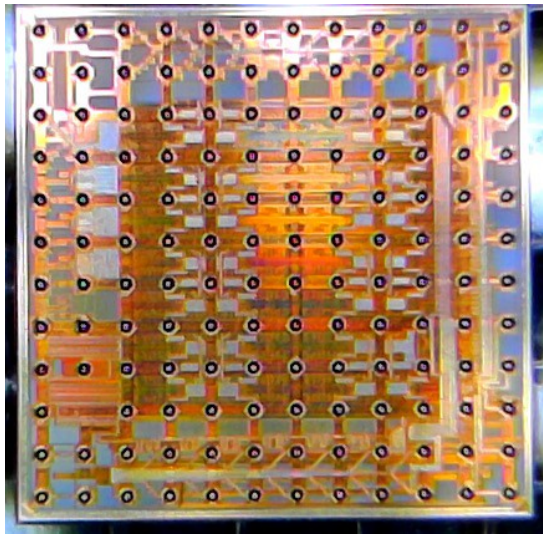
Control/readout circuits dominate consumption. Integration limited by **cryostat lift**

Equal1.lab 22nm FDSOI QPU for 4 K Operation

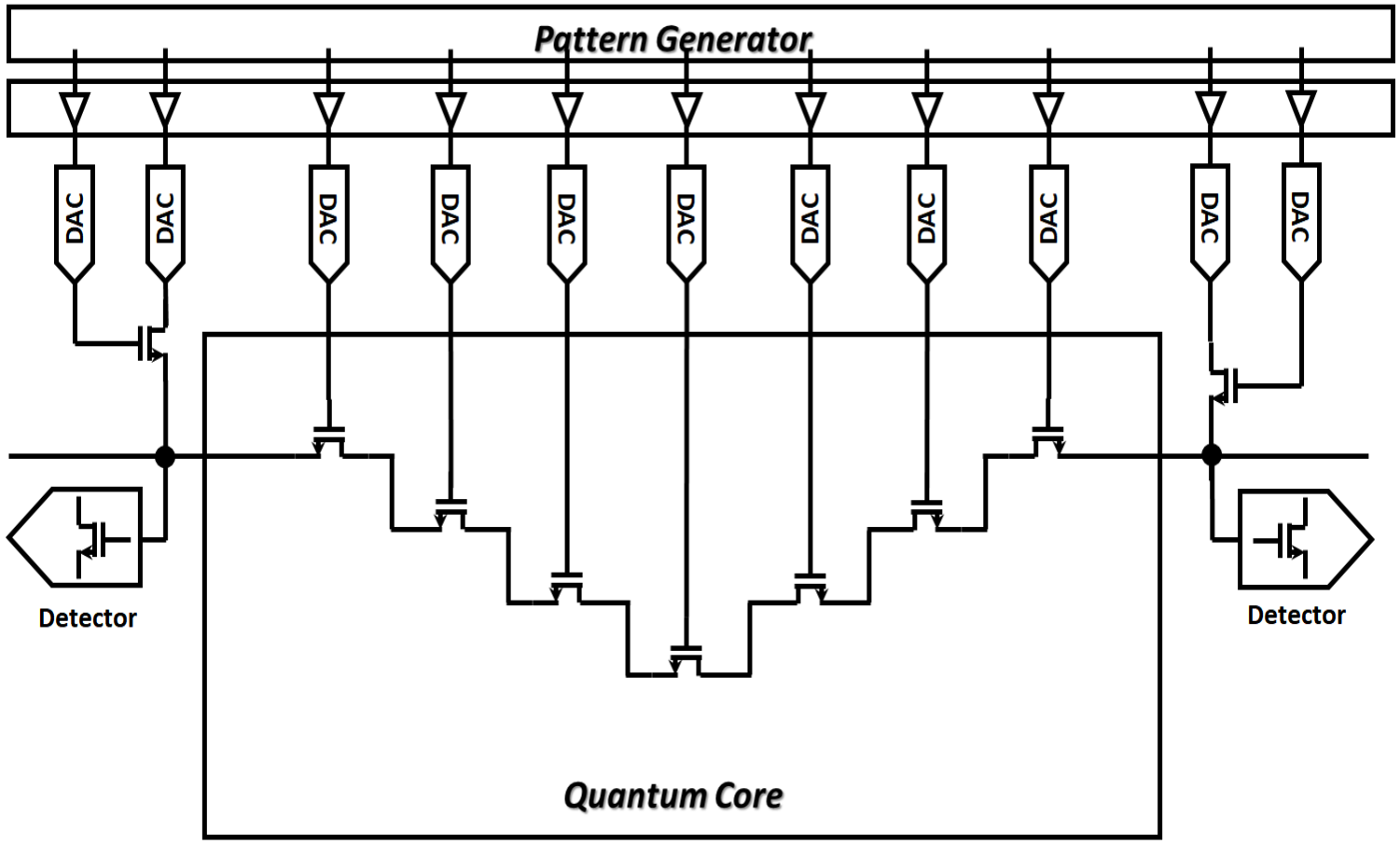


Fully-integrated SoC

- **Quantum**
- **Analog**
- **Mixed-signal**
- **Digital**

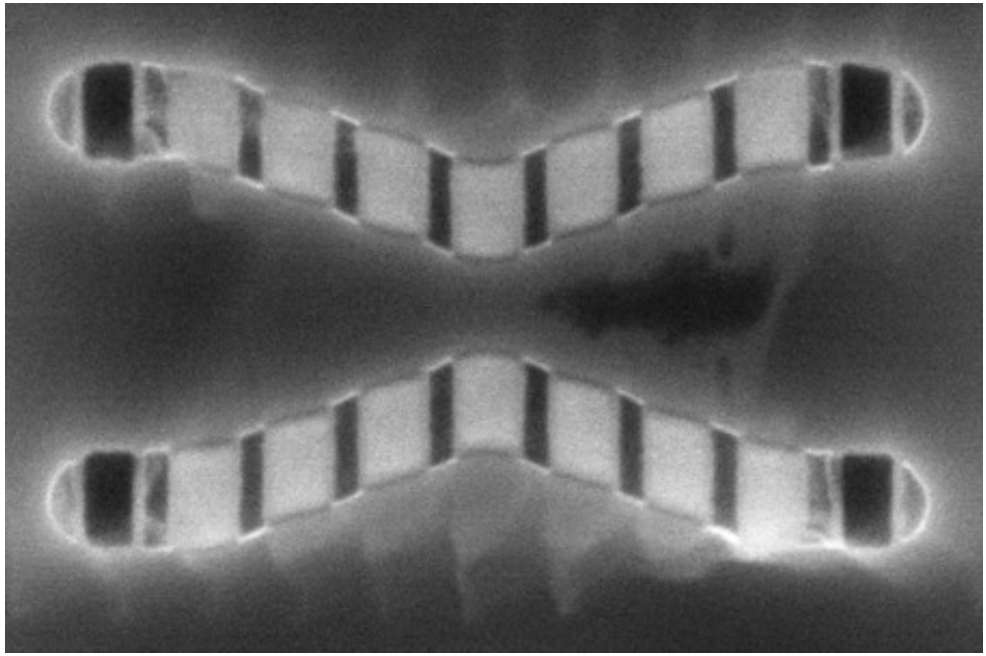


Equal1.lab 22nm FDSOI Quantum Core



Quantum structure & tightly integrated control & interface

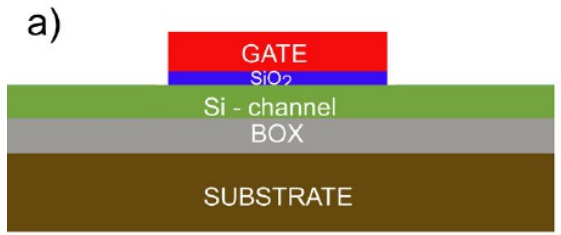
2D structure allows
Topological quantum computer

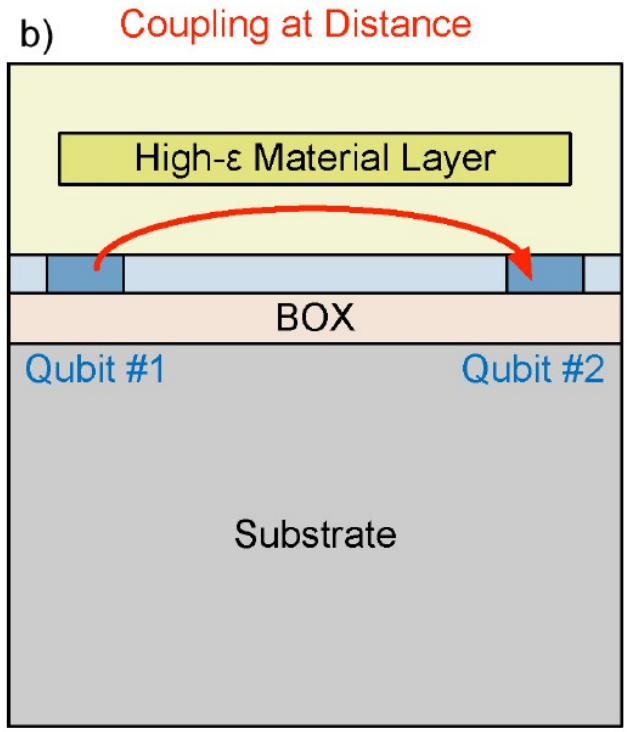


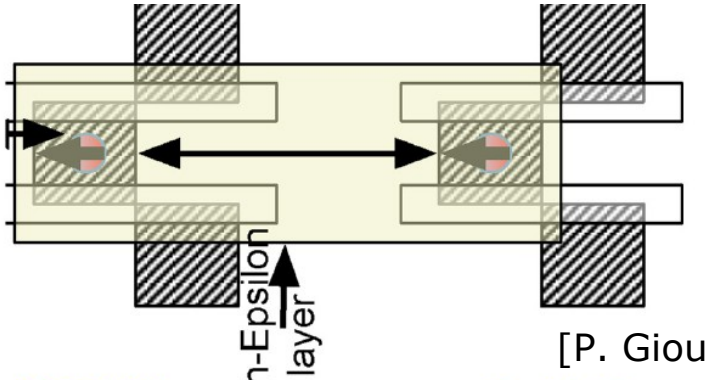
Patented quantum structures in customized GlobalFoundries FDX process

[D. Leipold, et al. 2019]

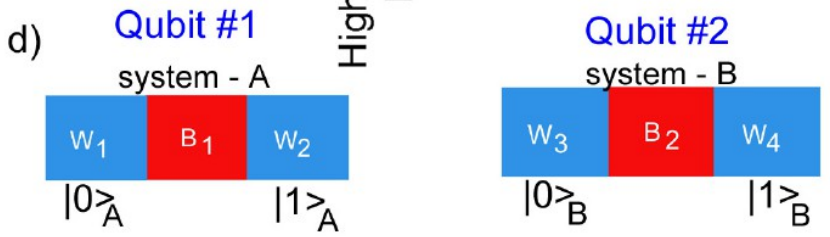
Photon-enhanced interaction/entanglement

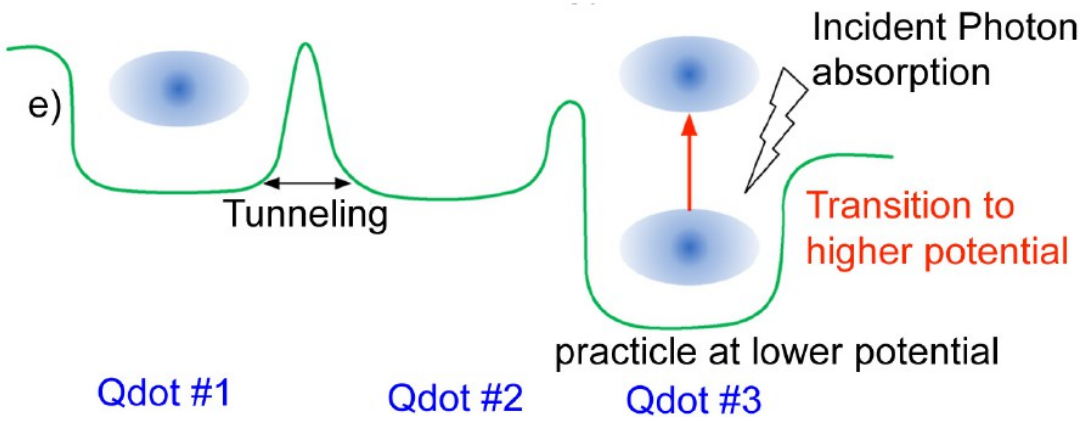






[P. Giounanlis et al. Appl.Sci. 2019]

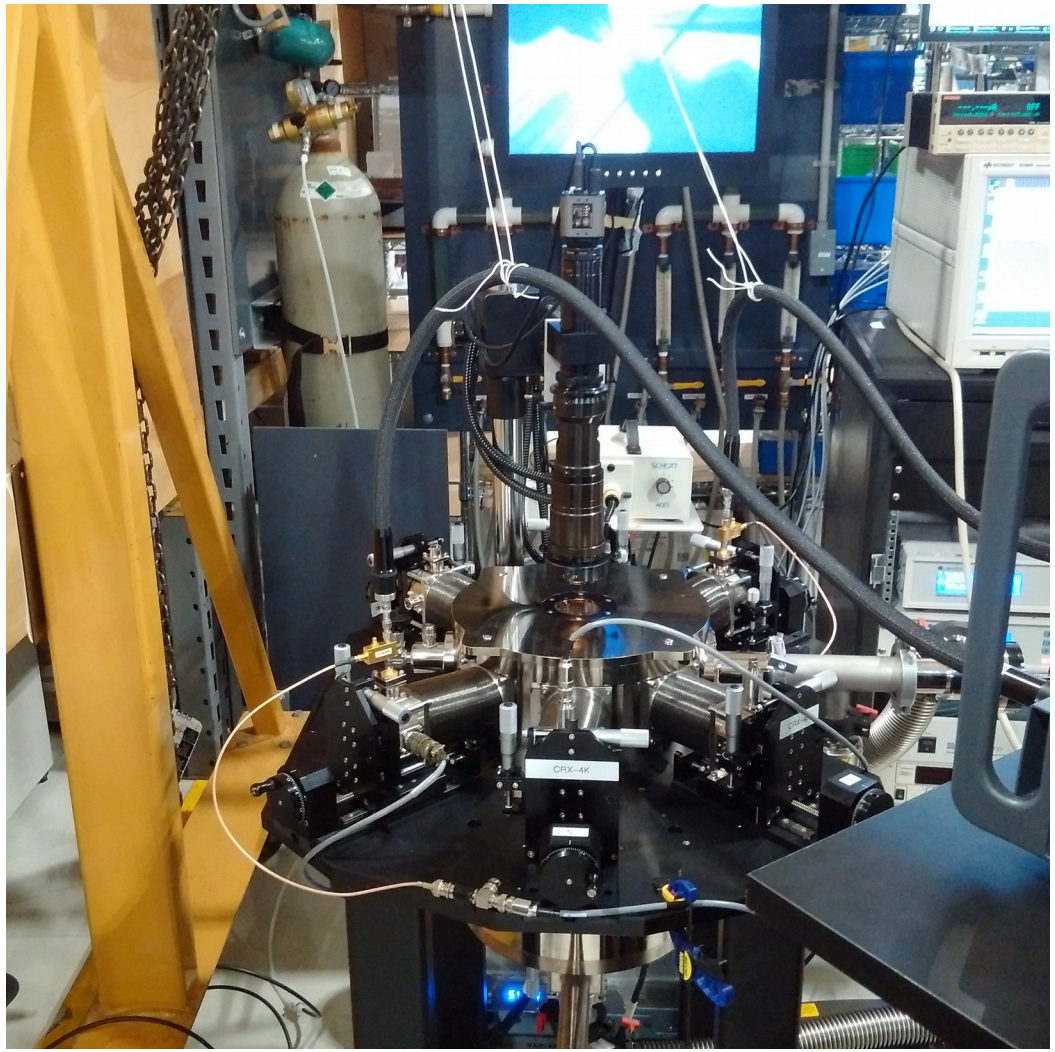


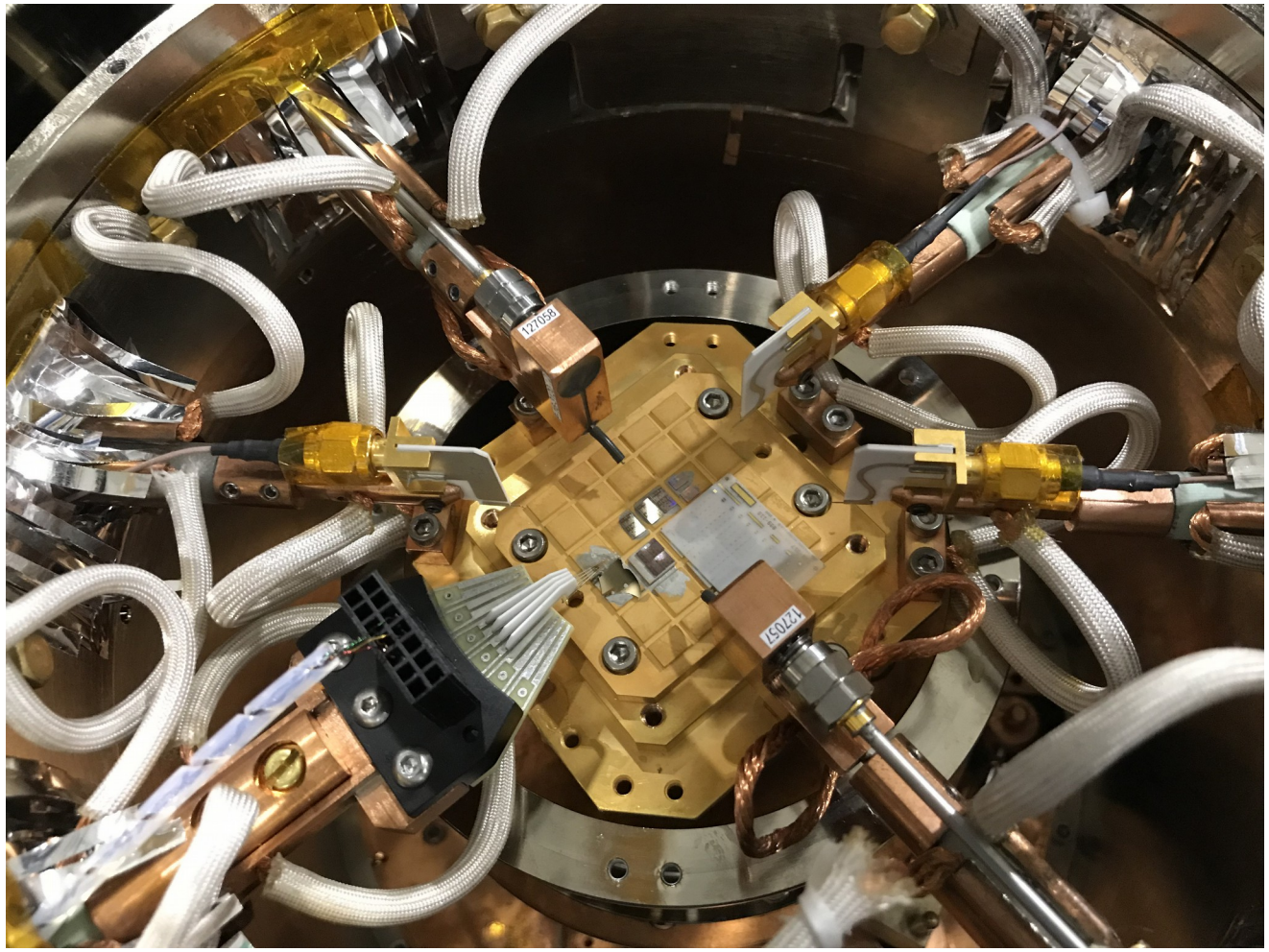


Outline

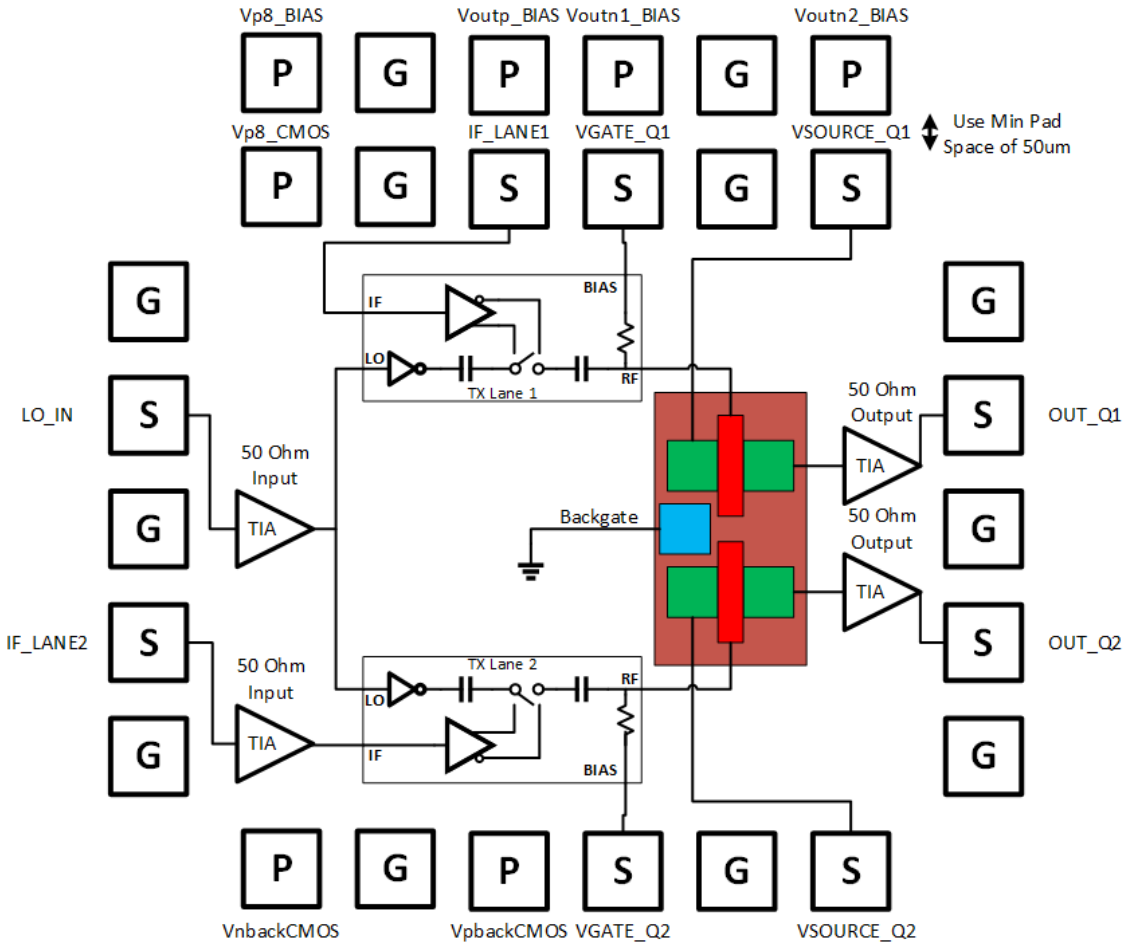
- Introduction
- Quantum Processor SoCs
- **Cryogenic characterization of 22nm FDSOI CMOS Technology**
- Conclusions

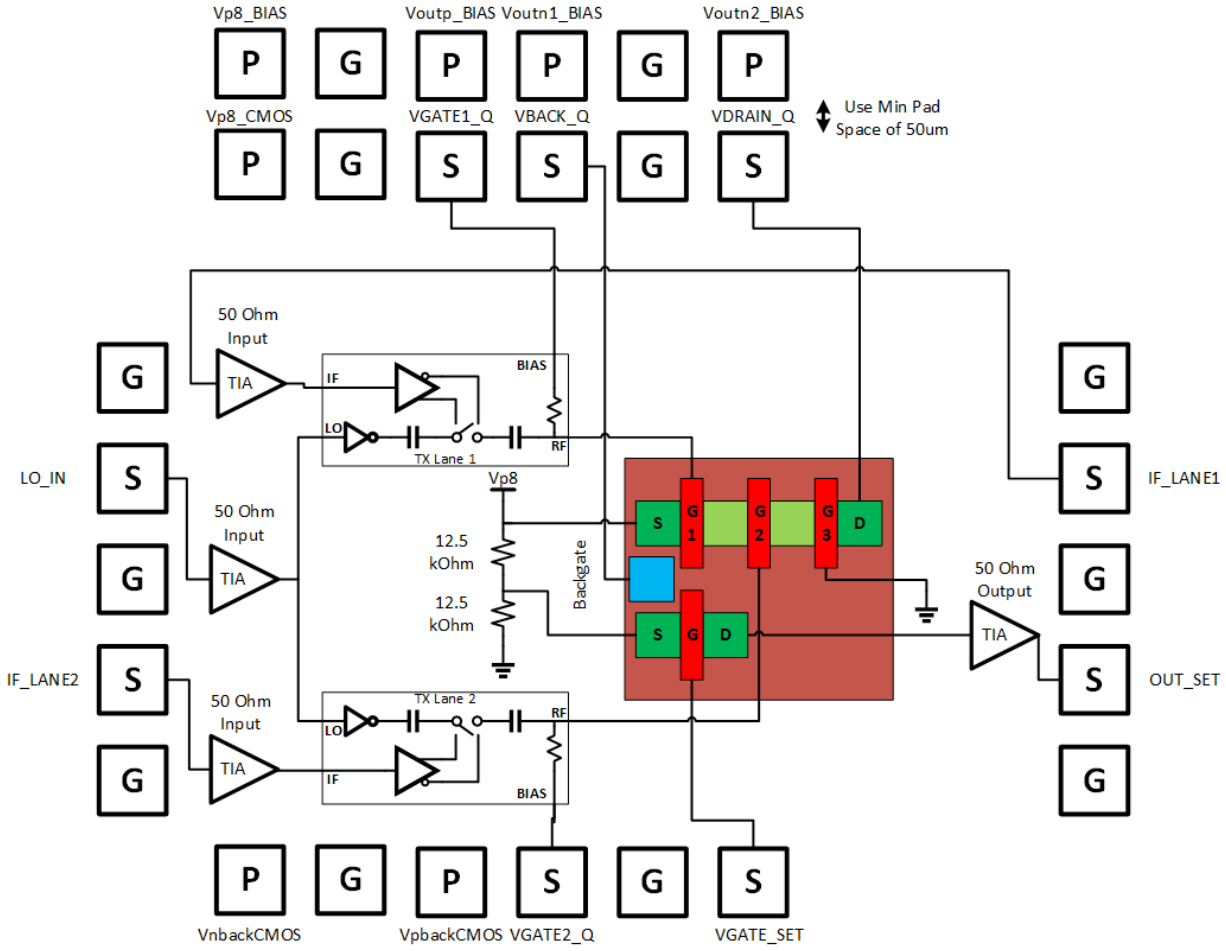
Measurement set-up at 2 K



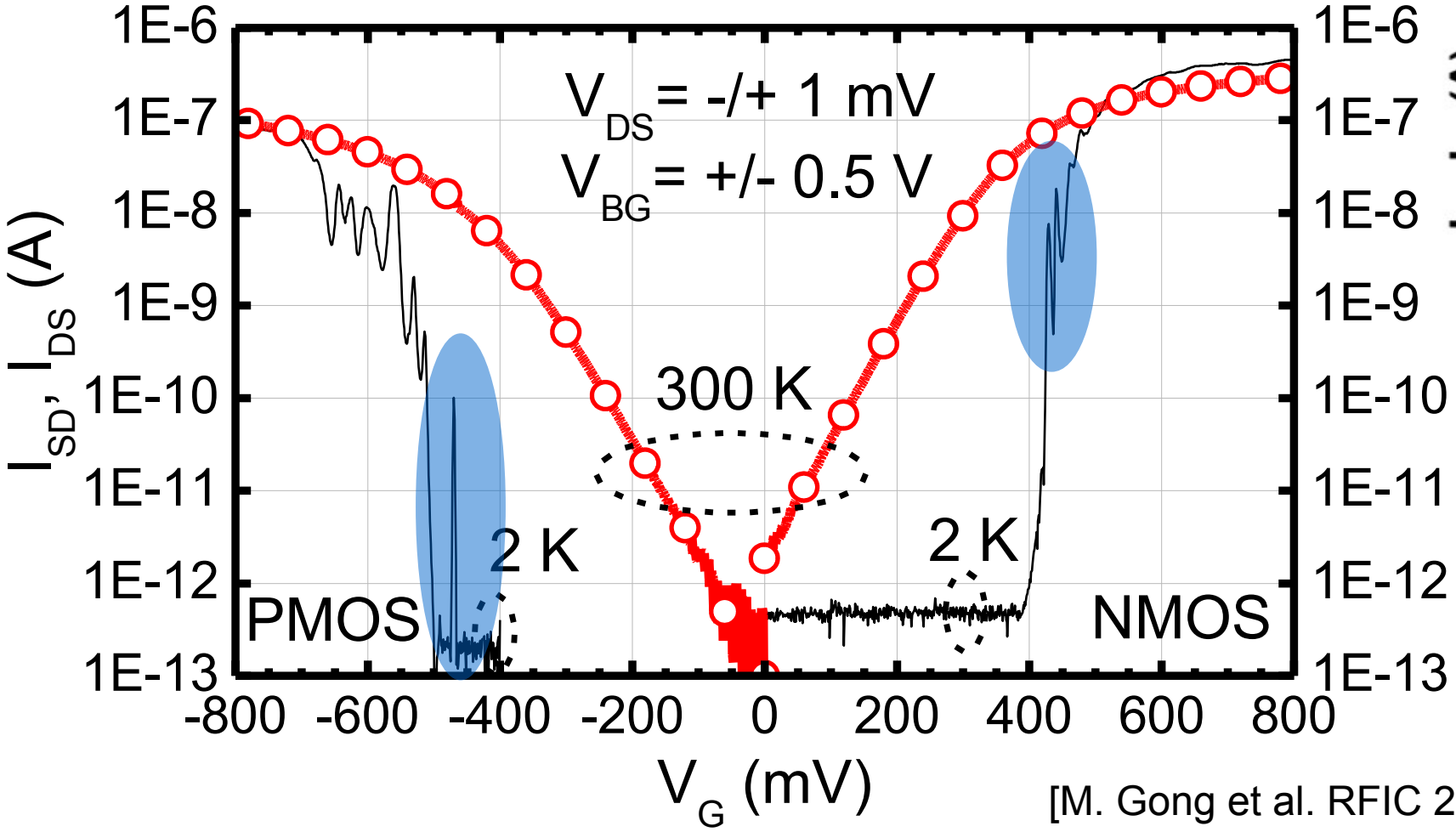


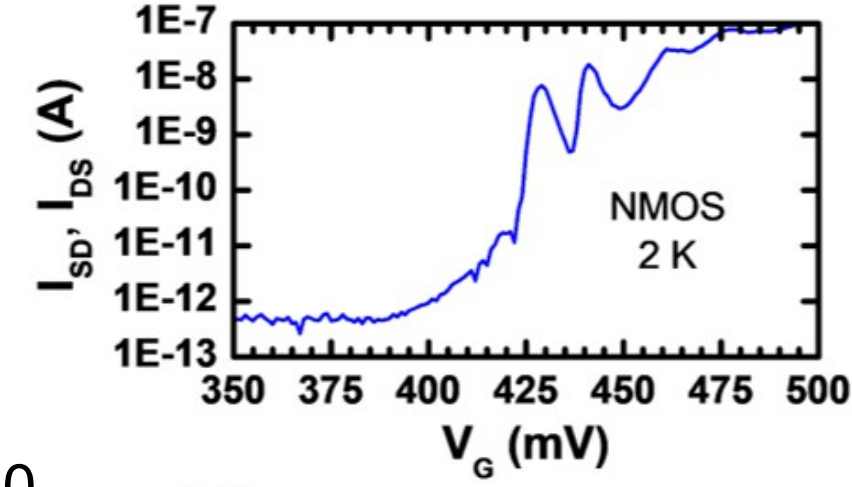
Die QPU testing limited by padframe, cryostat lift

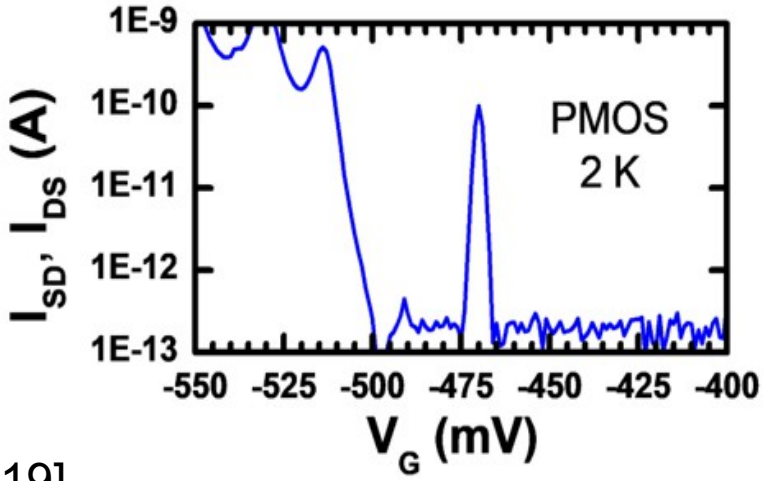




Quantum behavior at low V_{DS} and 2 K

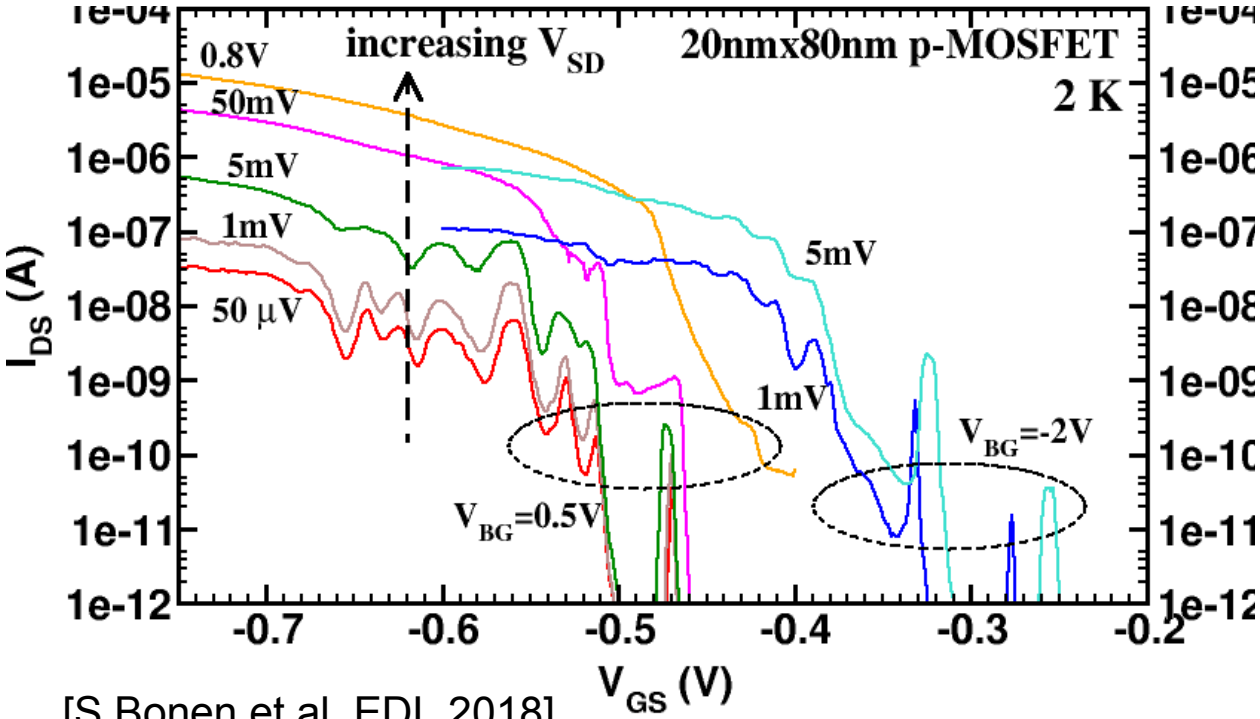


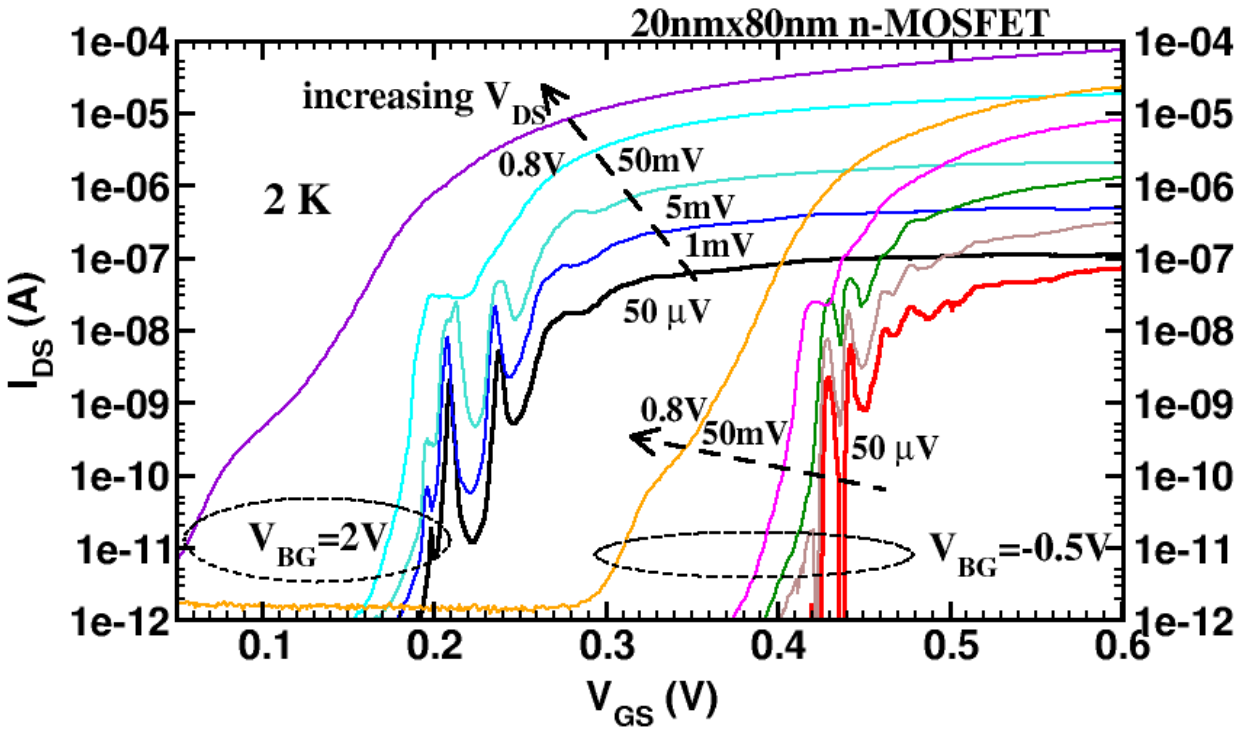




[M. Gong et al. RFIC 2019]

Energy level spacing tuneable from backgate

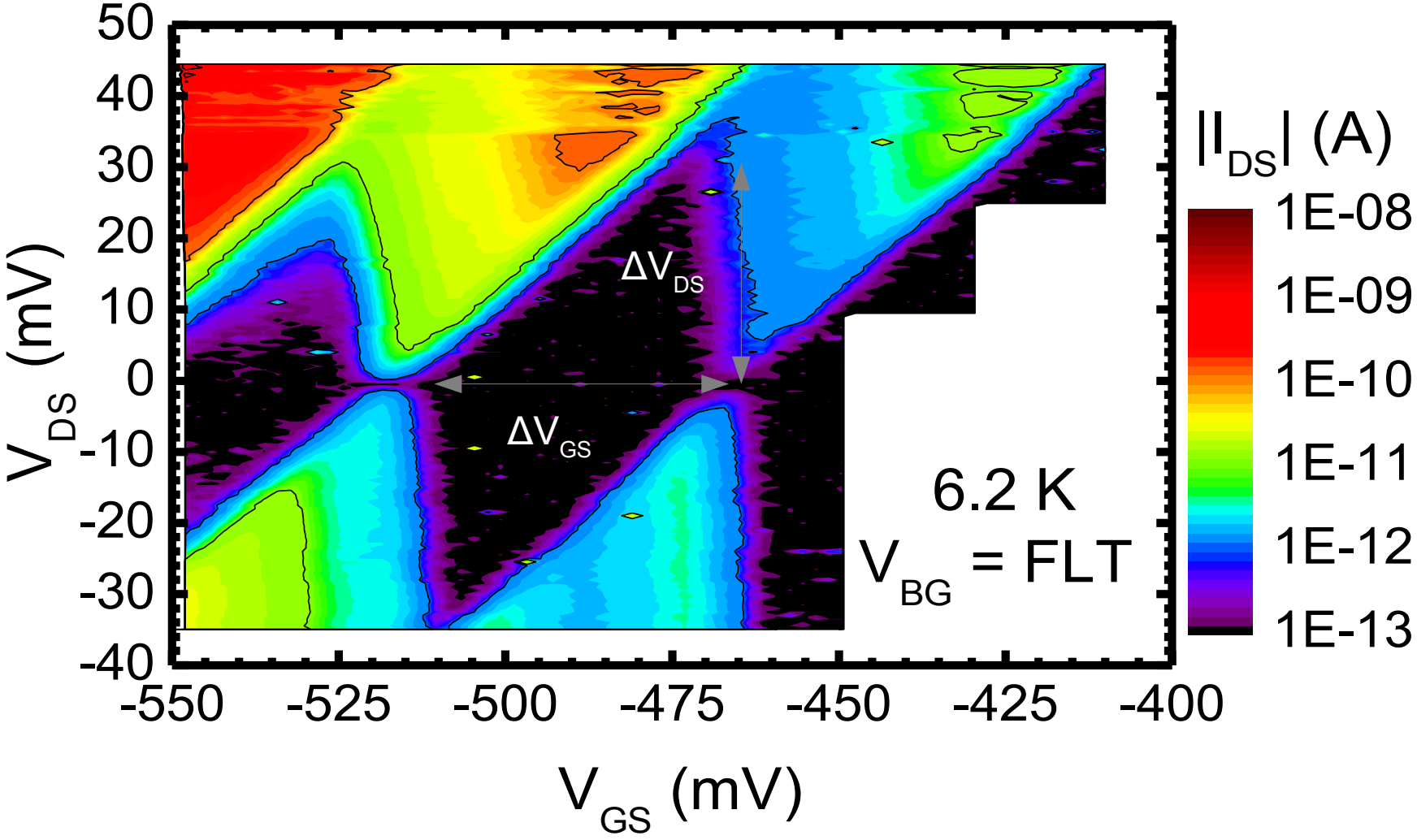




[S.Bonen et al. EDL 2018]

ΔV_{GS} increases (doubles) at +/-2V back gate voltage as C_{gs} decreases

18nmx70nm p-MOSFET: I_{DS} vs V_{GS} and V_{DS}



Sign of I_{DS} follows V_{DS}

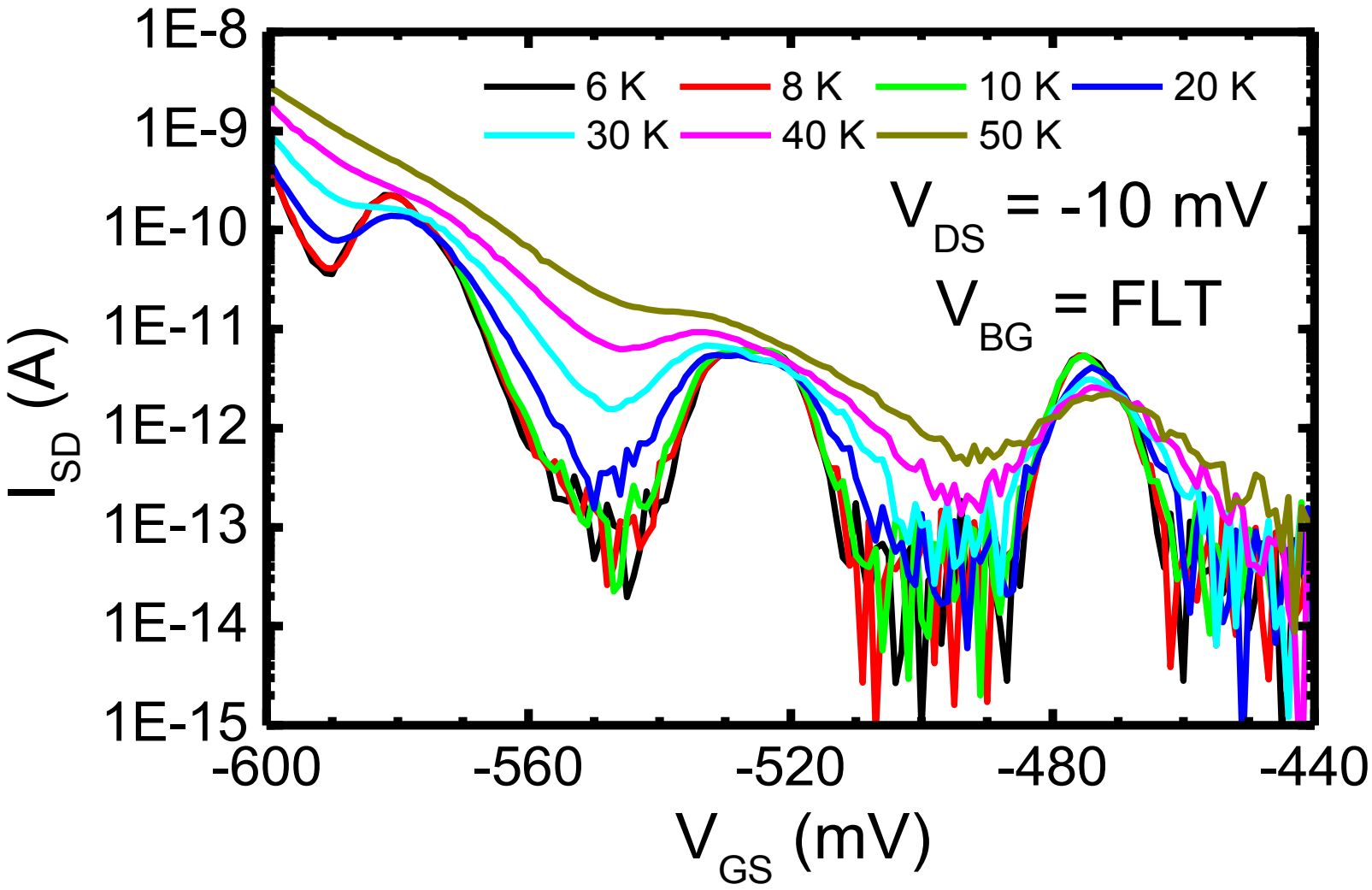
Operates like a single hole transistor (single electron transistor)

Regions of no current indicate bias regimes with integer number of trapped holes in the QD

"Diamonds" with large ΔV_{DS} indicate large $E_2 - E_1$. Estimate ~15 meV for this device

$E_2 - E_1$ limited by W = 70 nm

18nmx70nm p-MOSFET vs Temperature



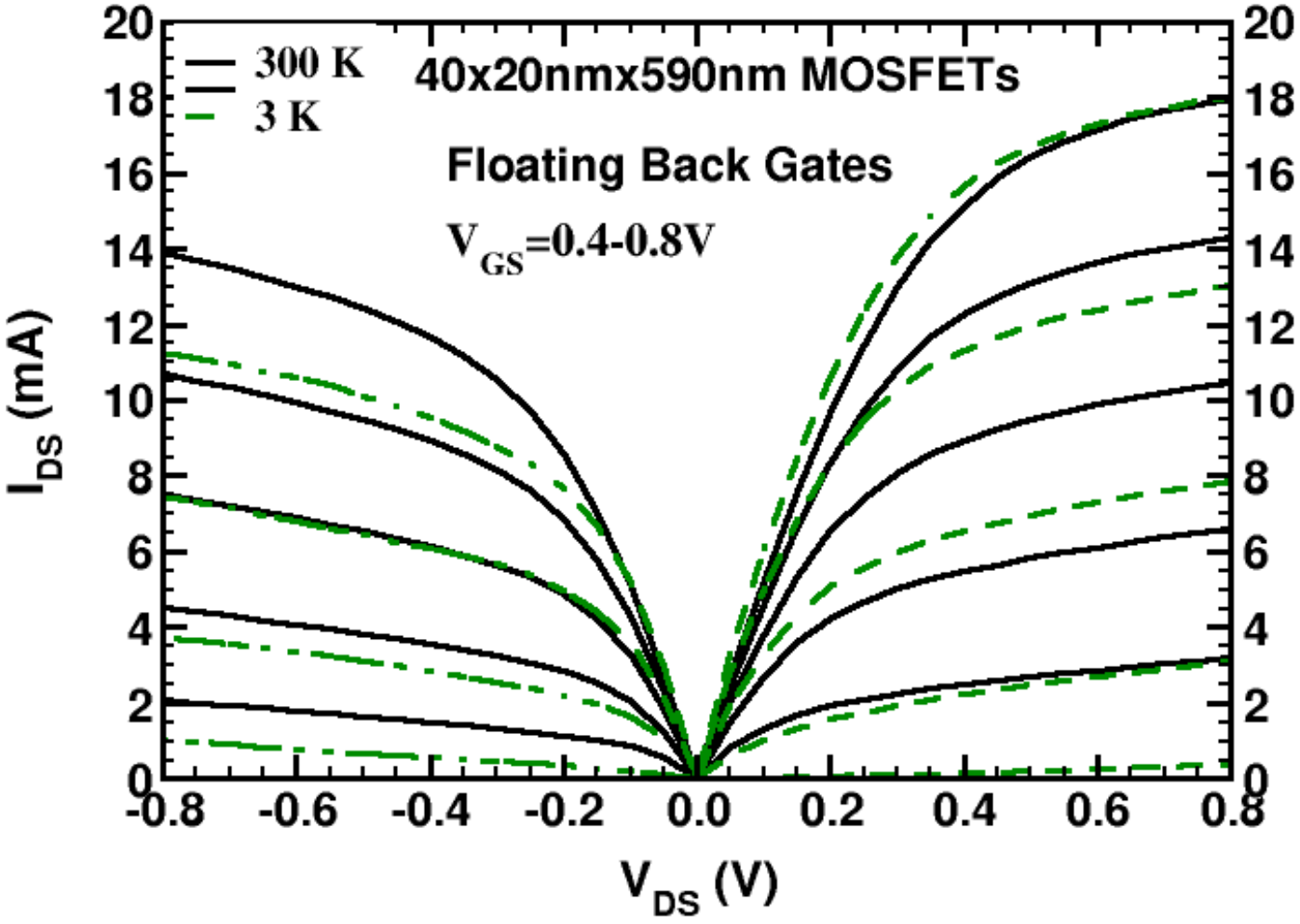
Resonant tunnelling current peaks widen over V_{GS} and decrease in $|I_{DS}|$ height as temperature increases

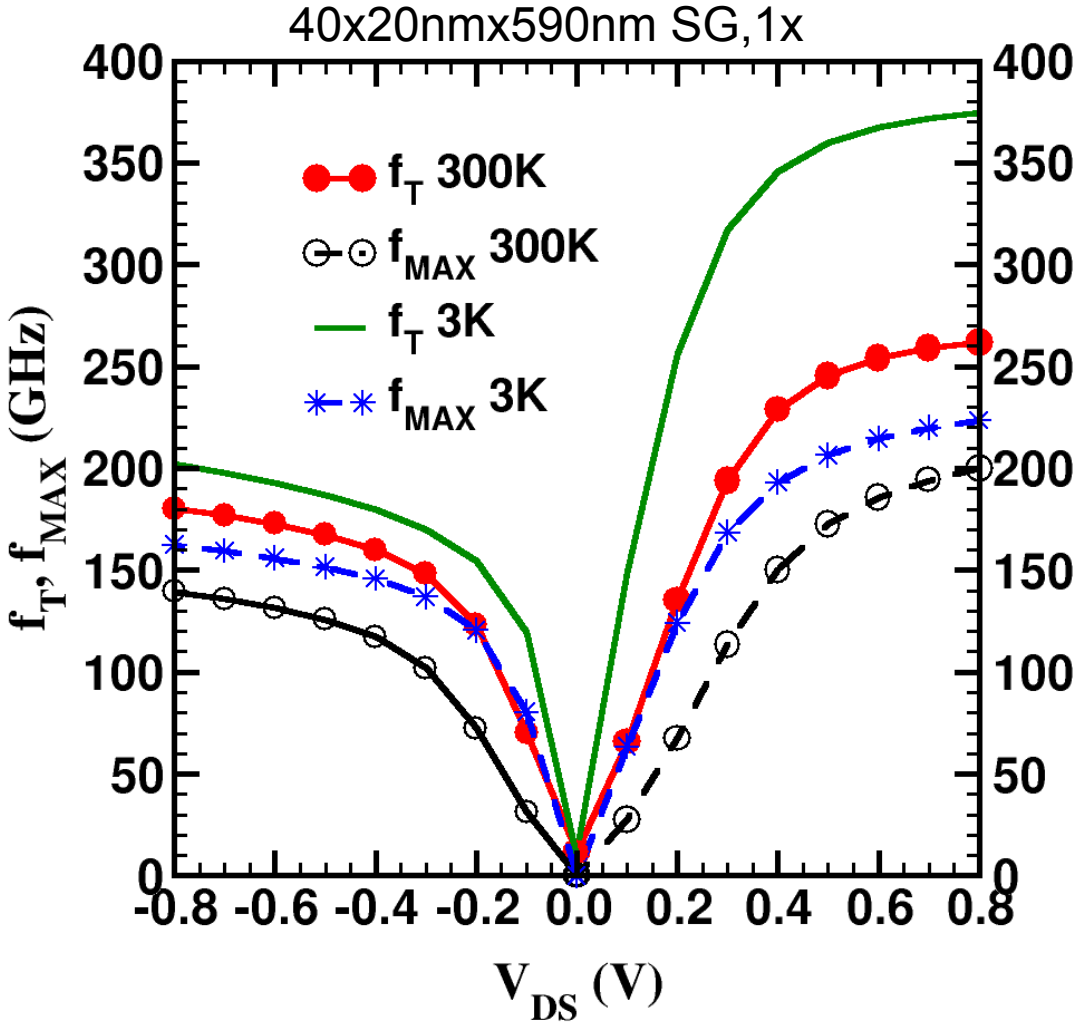
More thermionic emission overboth barriers of the QD as temperature increases

Qubit operation temperature scaling

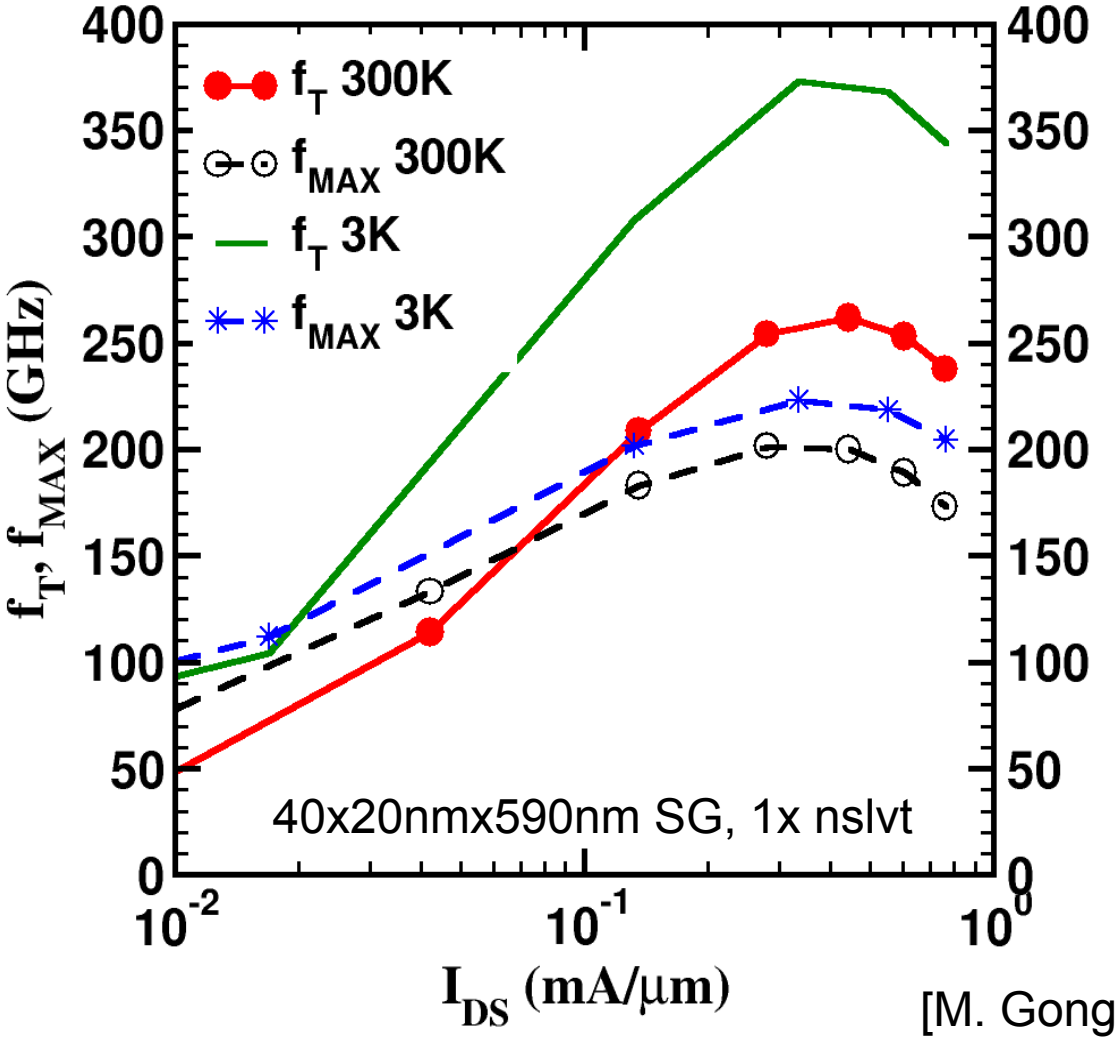
- f_L, T increase ~ L^{-2}, W^{-2} (very favourable scaling law)
- f_L, T increase linearly with dc magnetic field B_{dc}
  - B_{dc}=2.9T => ΔE_m=0.33meV, f_L=80.4 GHz, T=4 K, 22-nm FDSOI
  - B_{dc}=8.6T => ΔE_m=1meV, f_L=241.2 GHz, T=12 K, 12-nm feature?
  - B_{dc}=17.3T => ΔE_m=2meV, f_L=582.4 GHz, T=24 K, SiGe BiCMOS?
- Magnetic field and double-dot coupling energy limit T, f_L
  - Higher gyromagnetic factor helps => hole spin in SiGe channel

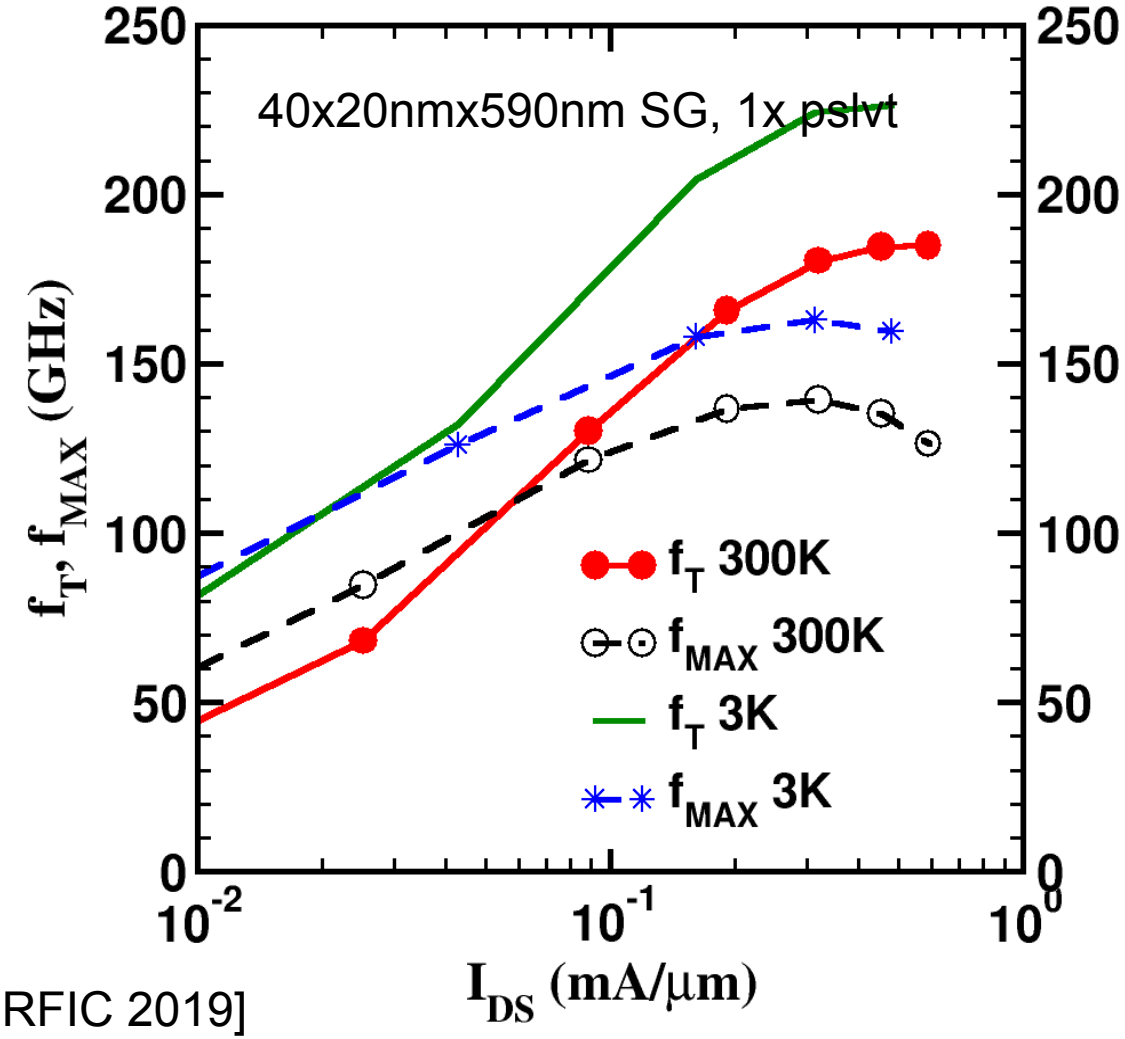
“Classical” MOSFET behaviour in saturation





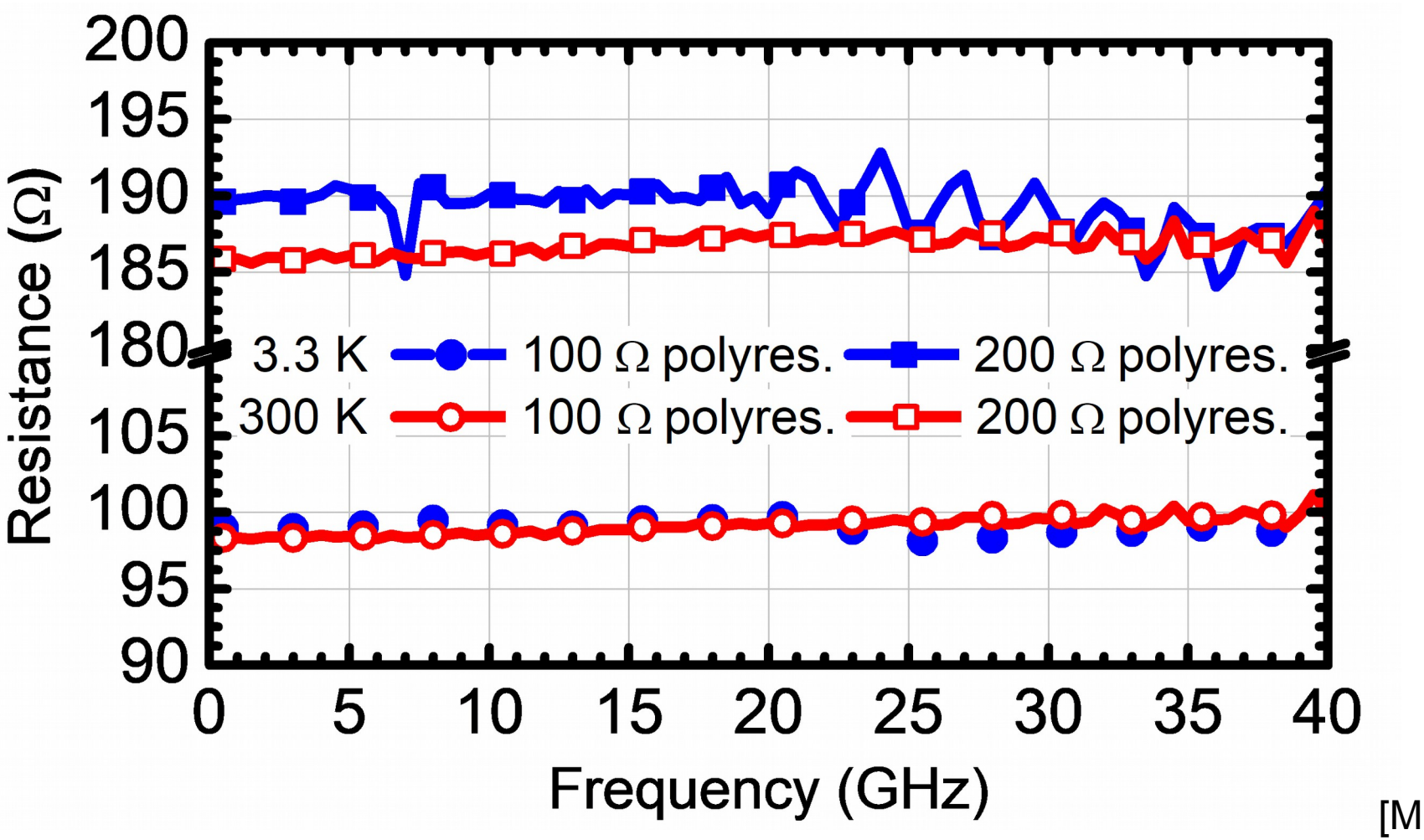
Peak f_T, f_{MAX} current densities invariant with temp.





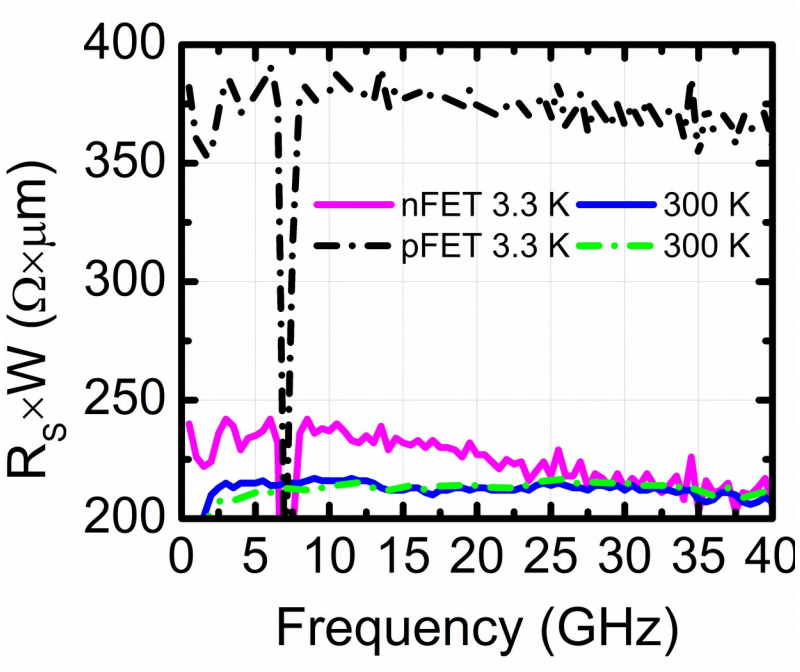
[M. Gong et al. RFIC 2019]

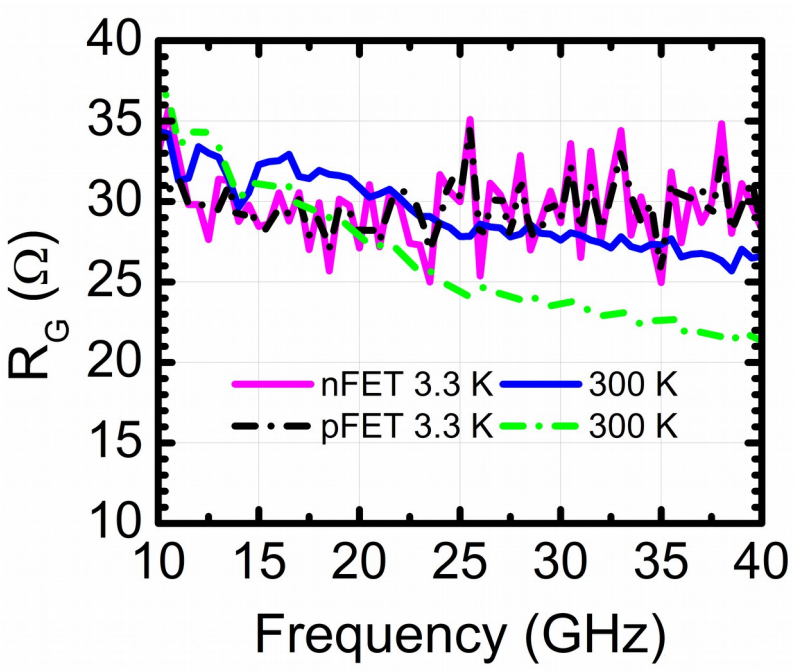
R_{poly} does not change over temperature

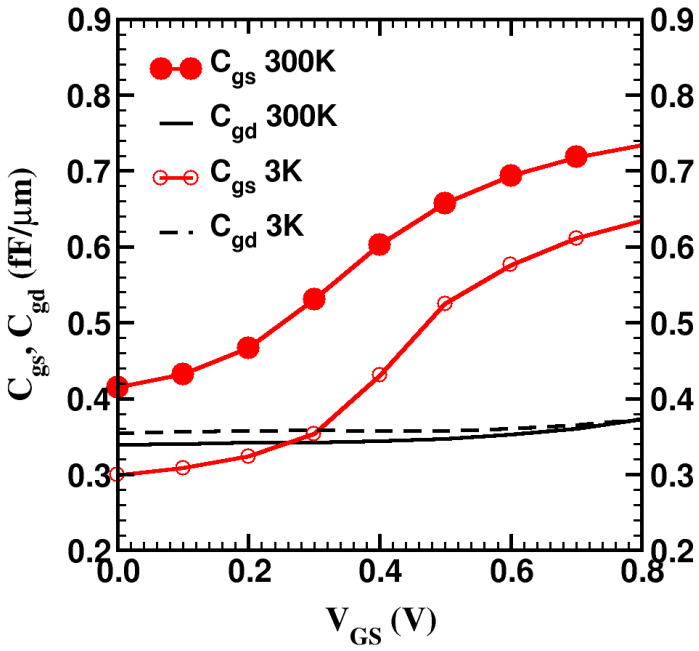


[M. Gong et al. RFIC 2019]

Parameter extraction at 2-3 K



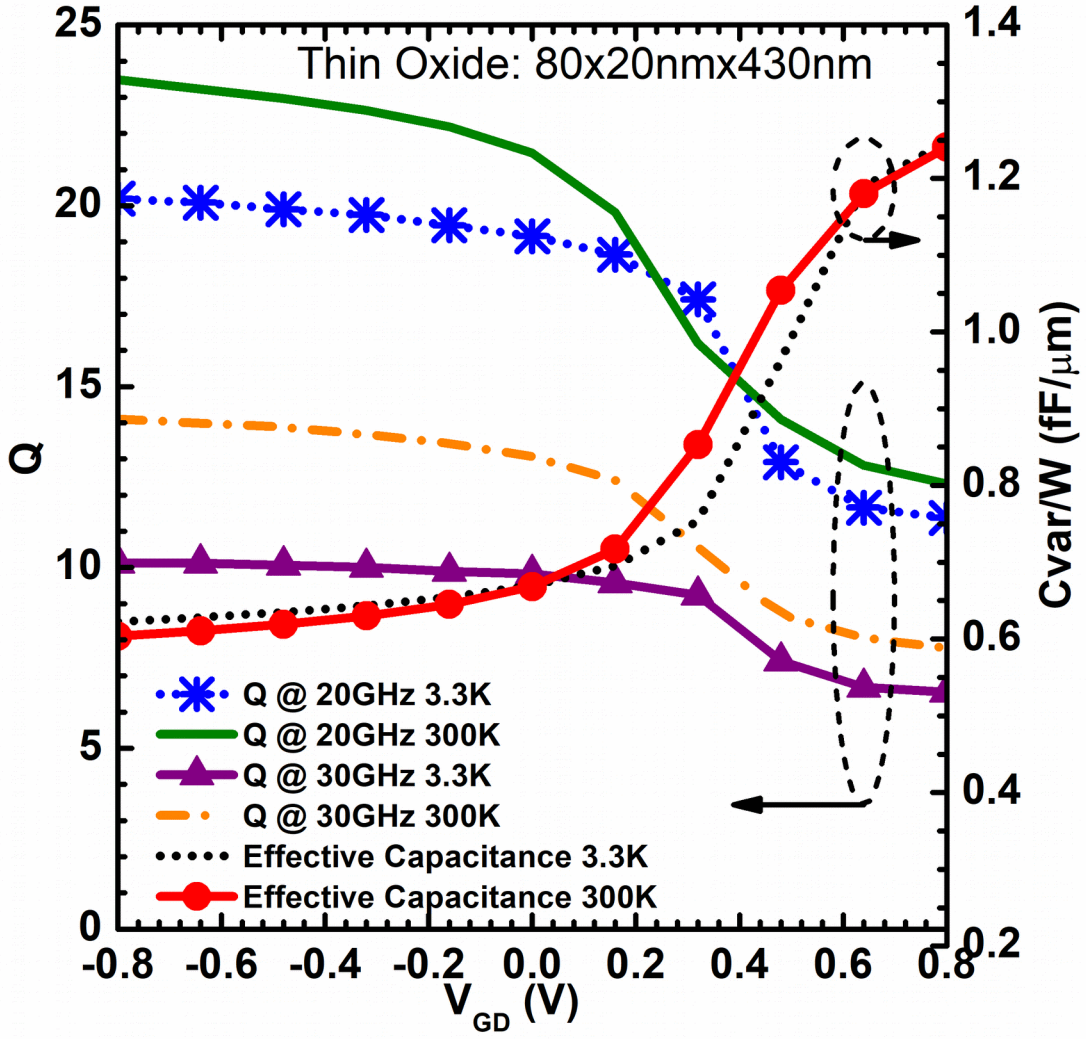


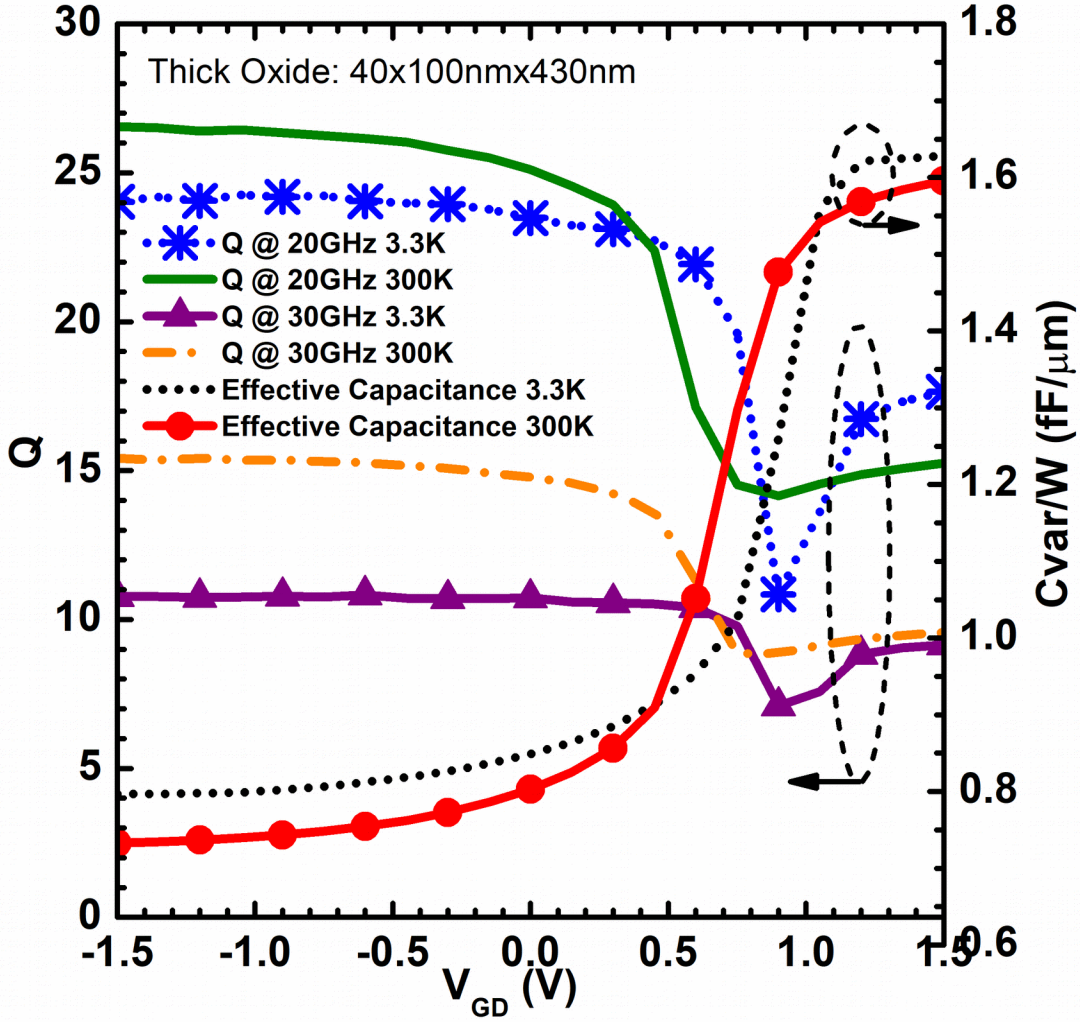


[M.J. Mecca et al. RFIC 2019]

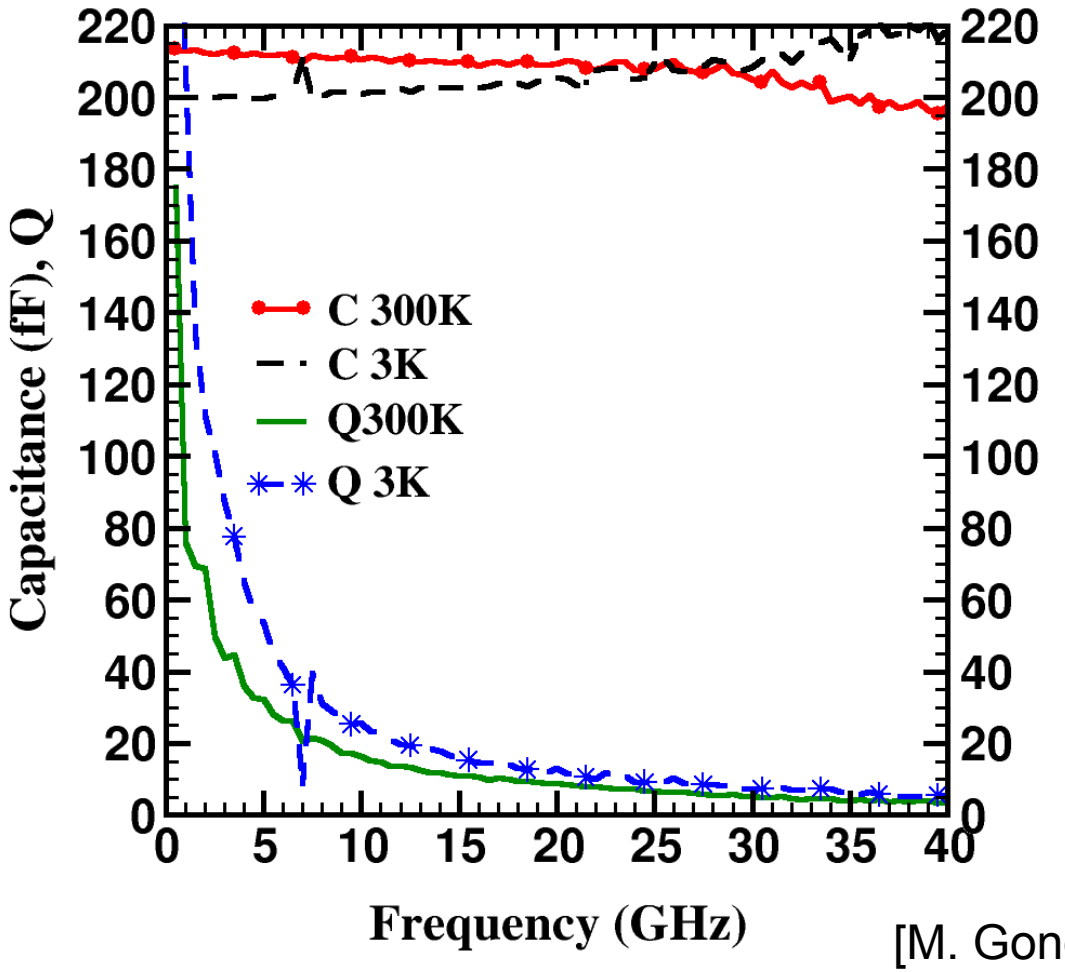
- Need on-die calibration in 2 K mm-wave probe station (with magnetic field)
- Source/drain resistance confirms different barriers for p- and n-MOSFET

Thick and Thin-Oxide Varactors: Q degrades

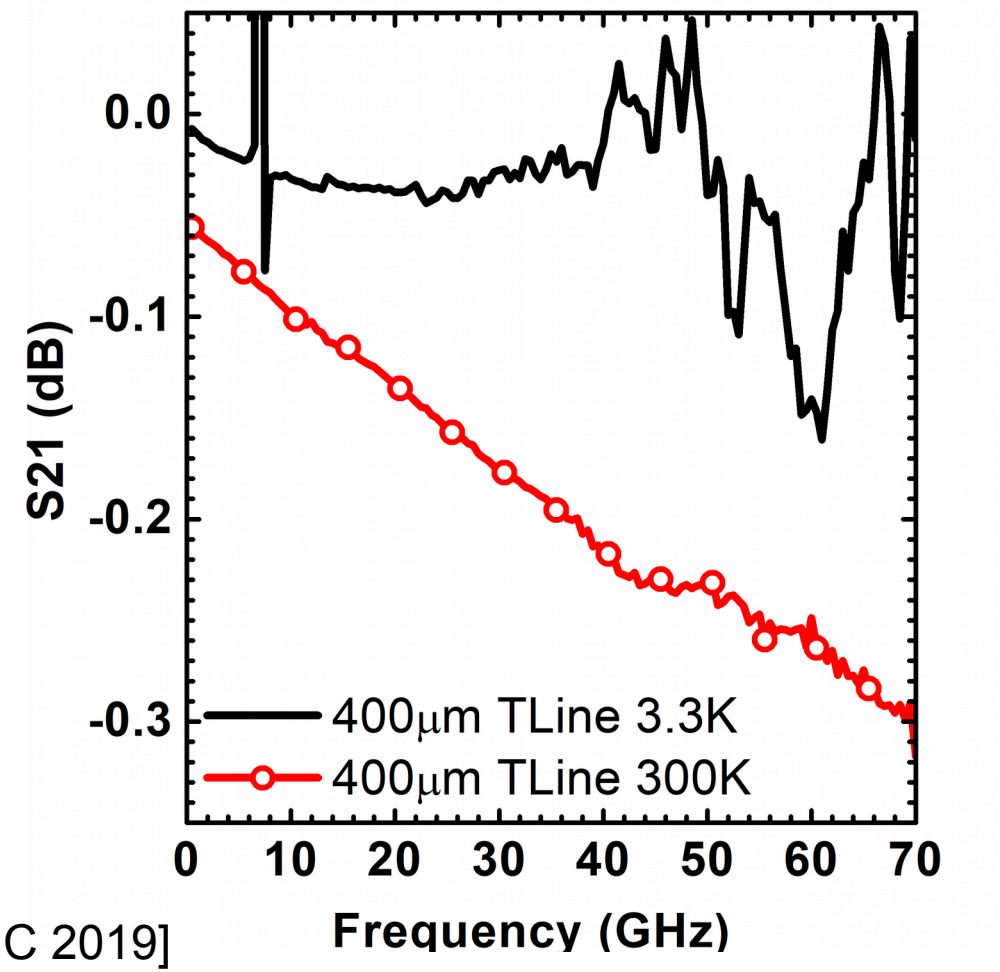




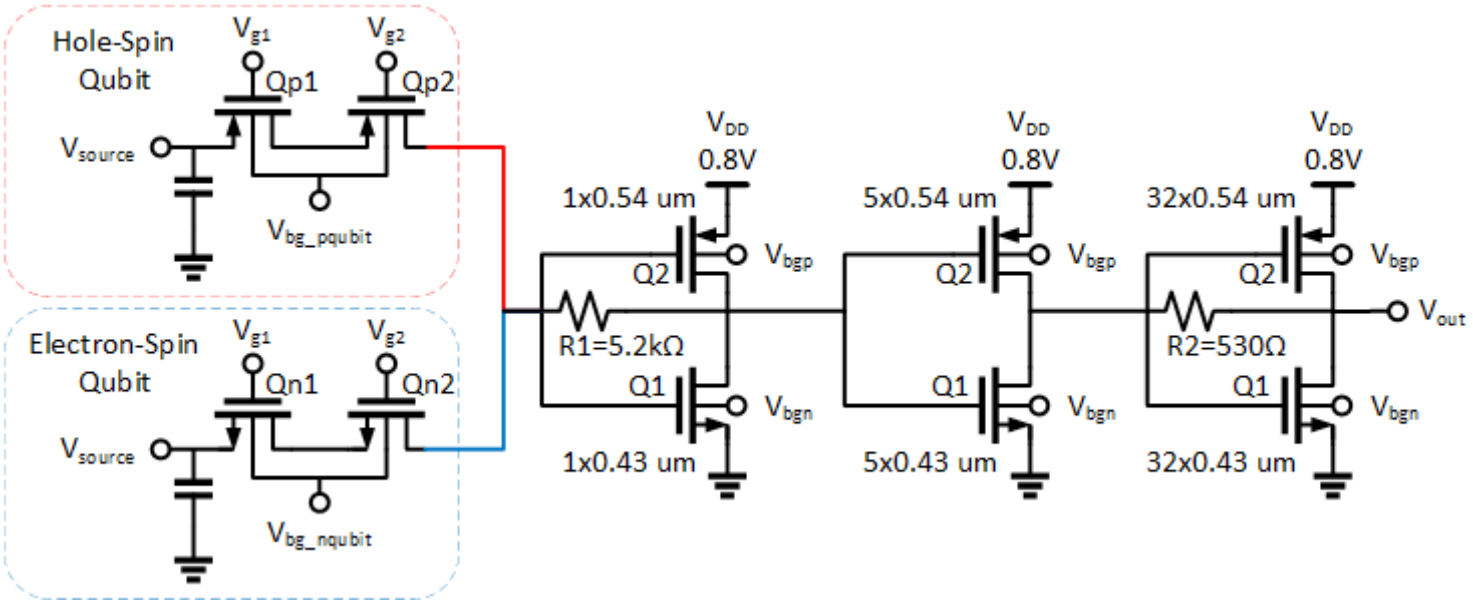
MoM Cap does not change but Q improves at 3 K

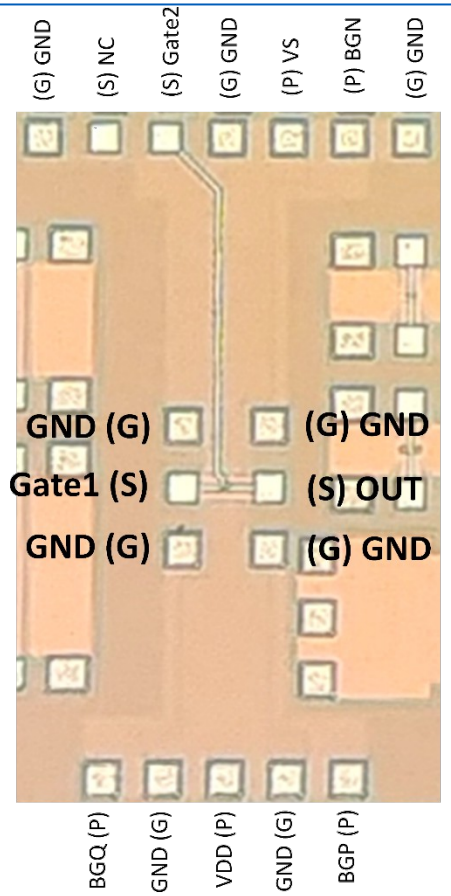


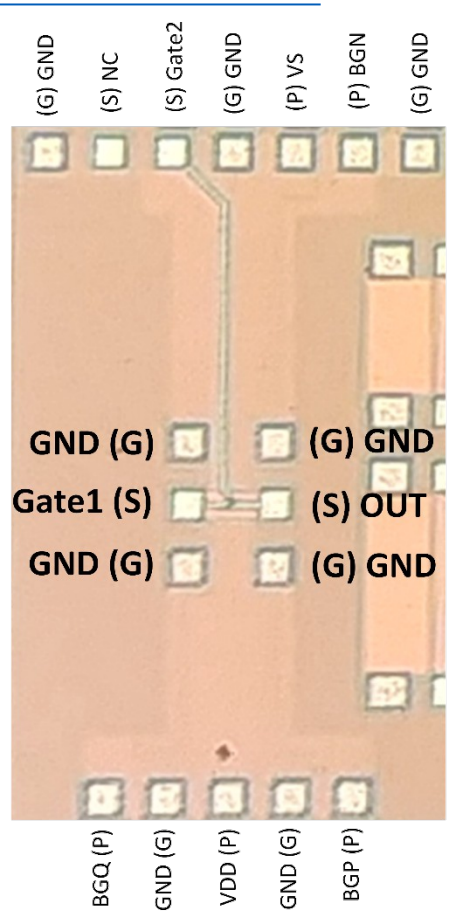
[M. Gong et al. RFIC 2019]



Monolithic integration of qubits and readout TIA







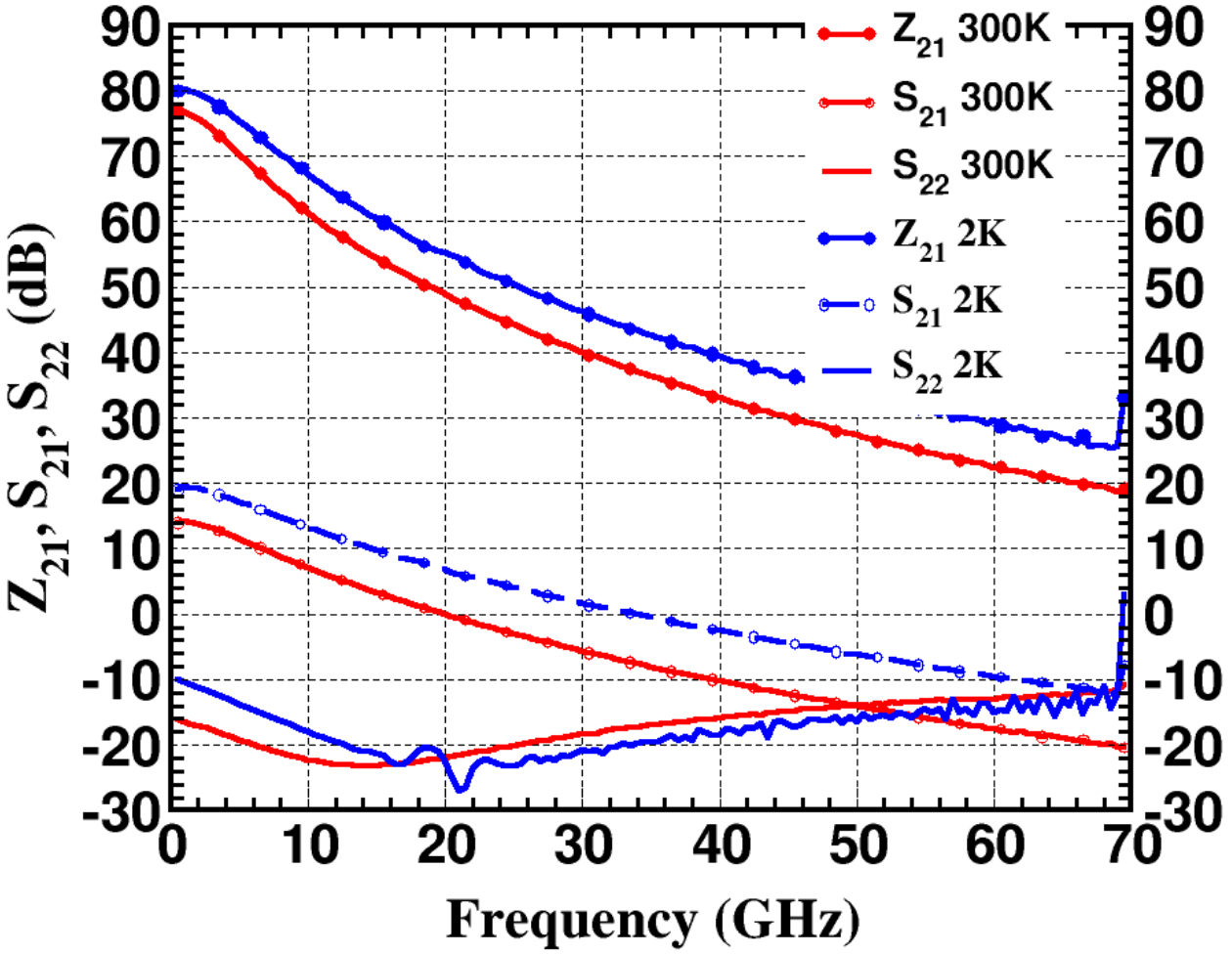
Challenges:

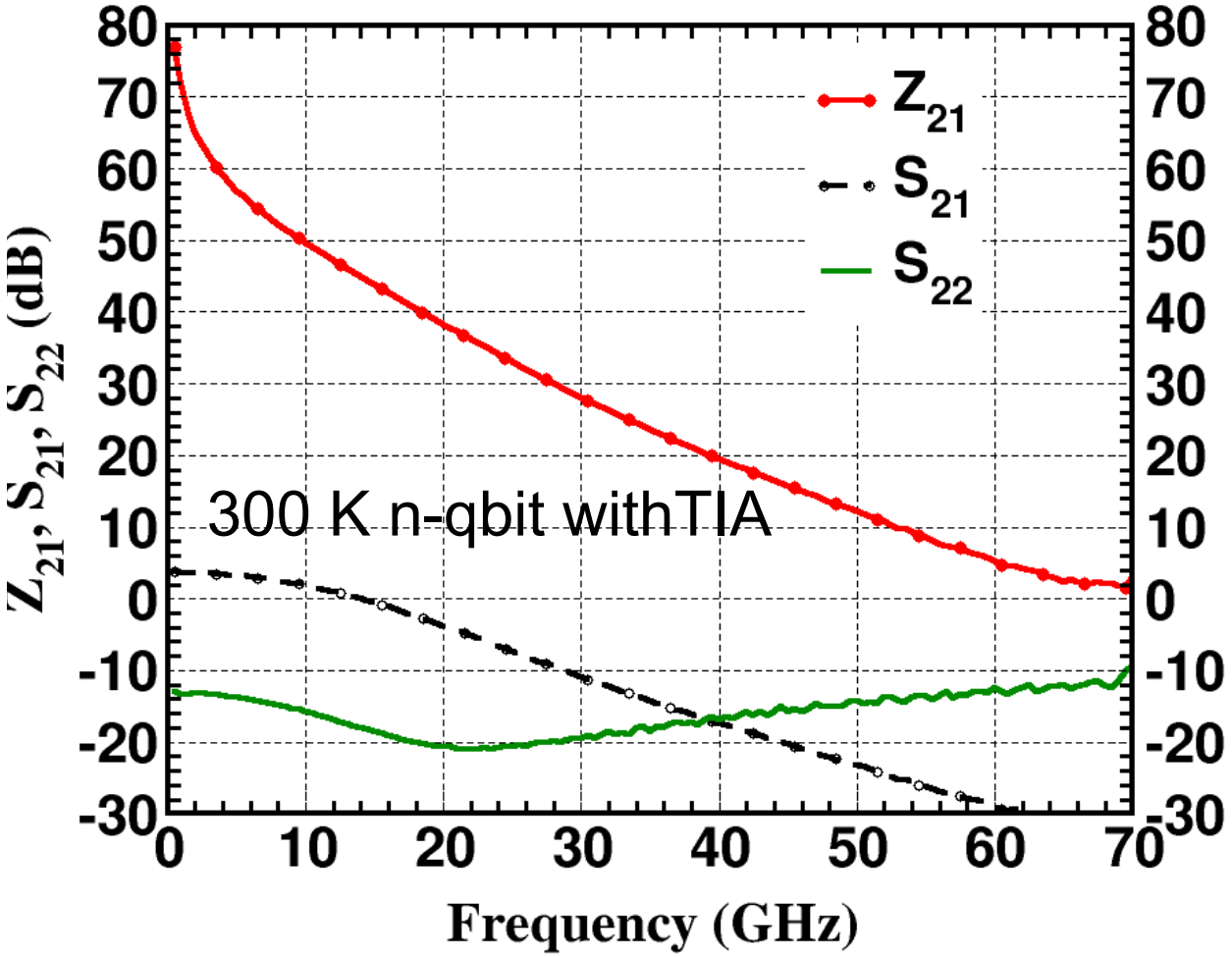
- Large gain, low power
- Bandwidth, noise
- Drive 50 Ω off chip with minimum size 1x18nmx70nm MOSFET
- Design kit models valid at 2-4 K

TIA and n-qubit+readout circuit vs. temperature

TIA

[S.Bonen et al. EDL 2018]

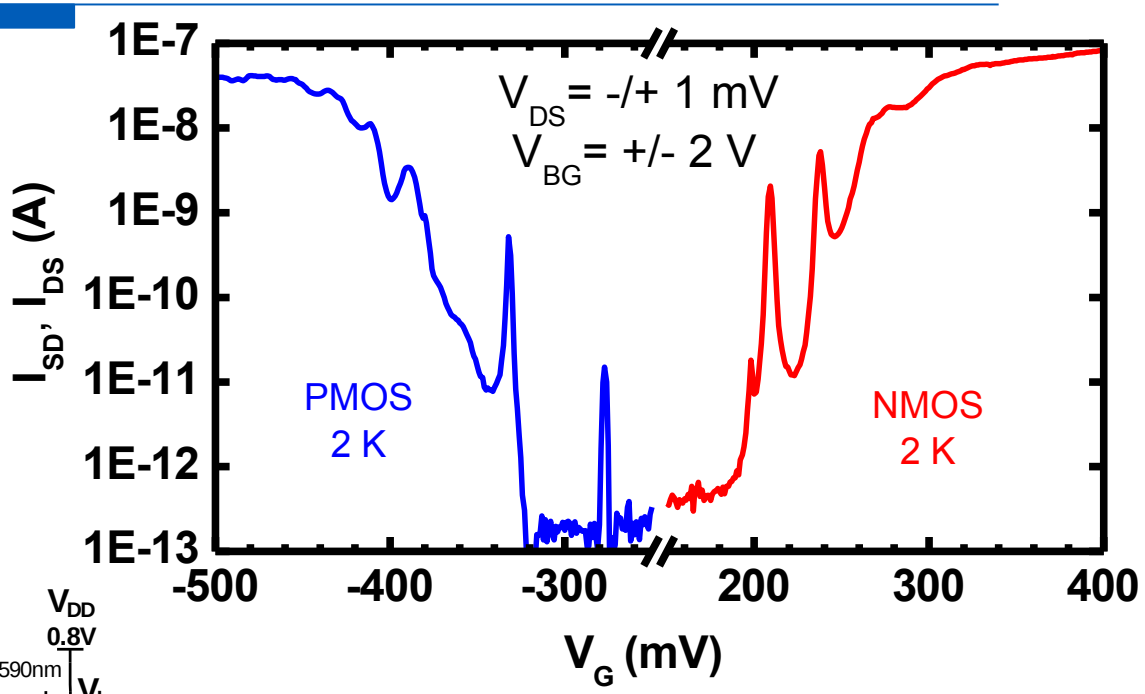


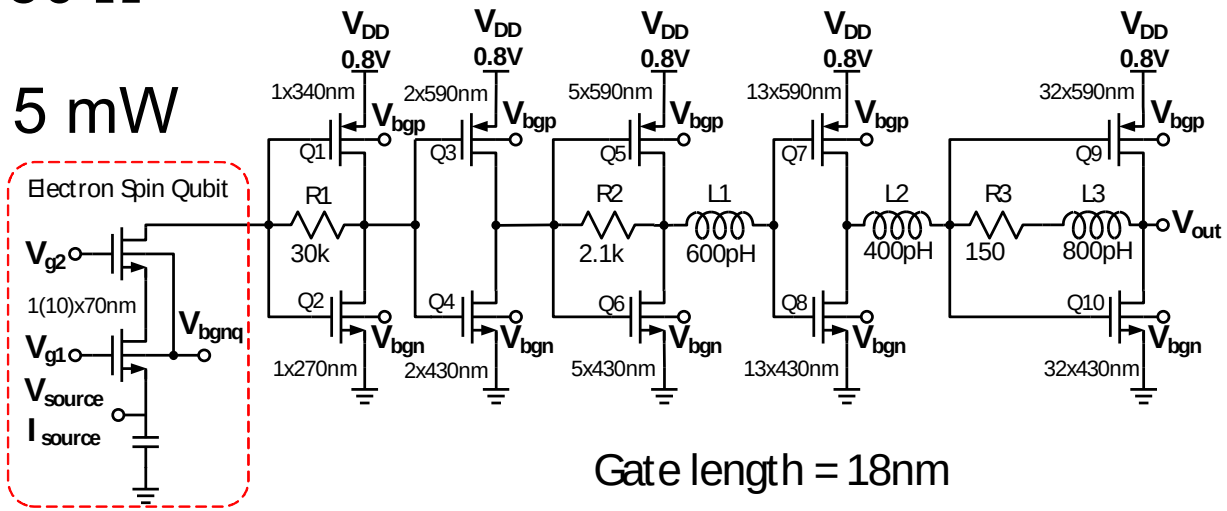


Specification and optimal TIA design for readout

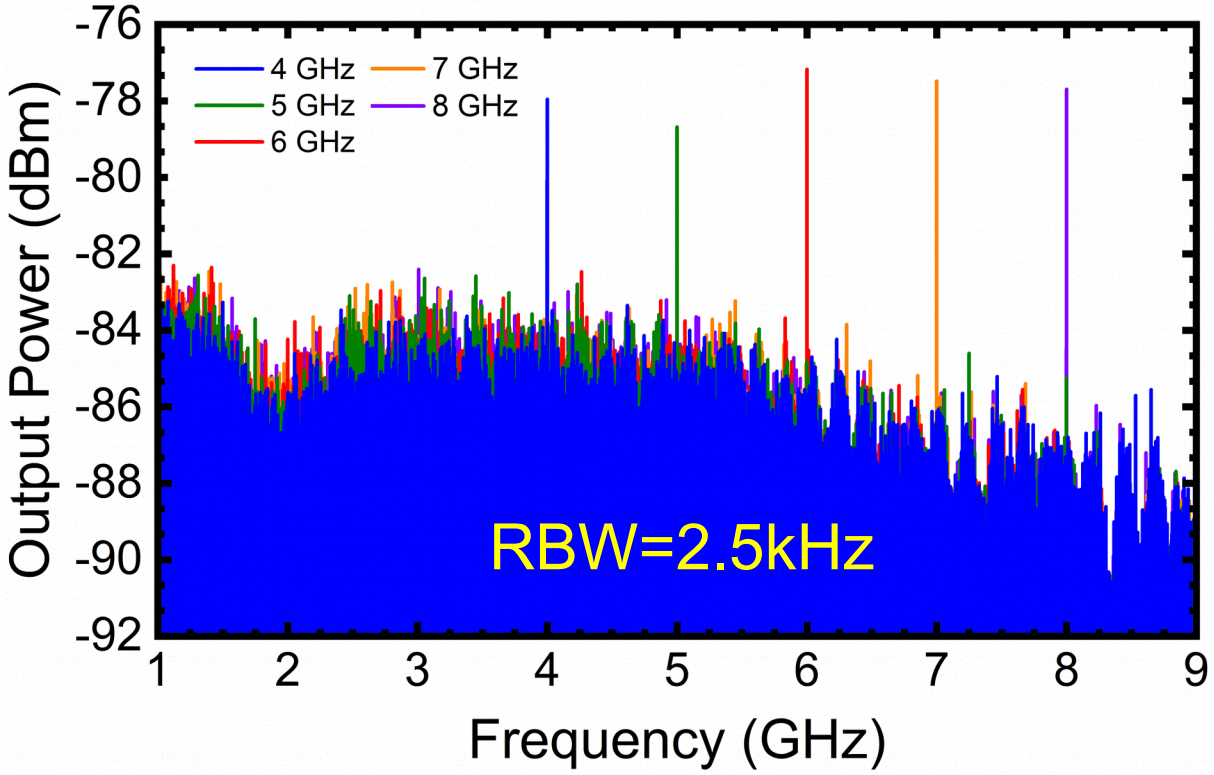
- Amplify 1pA...1nA to 10 mV

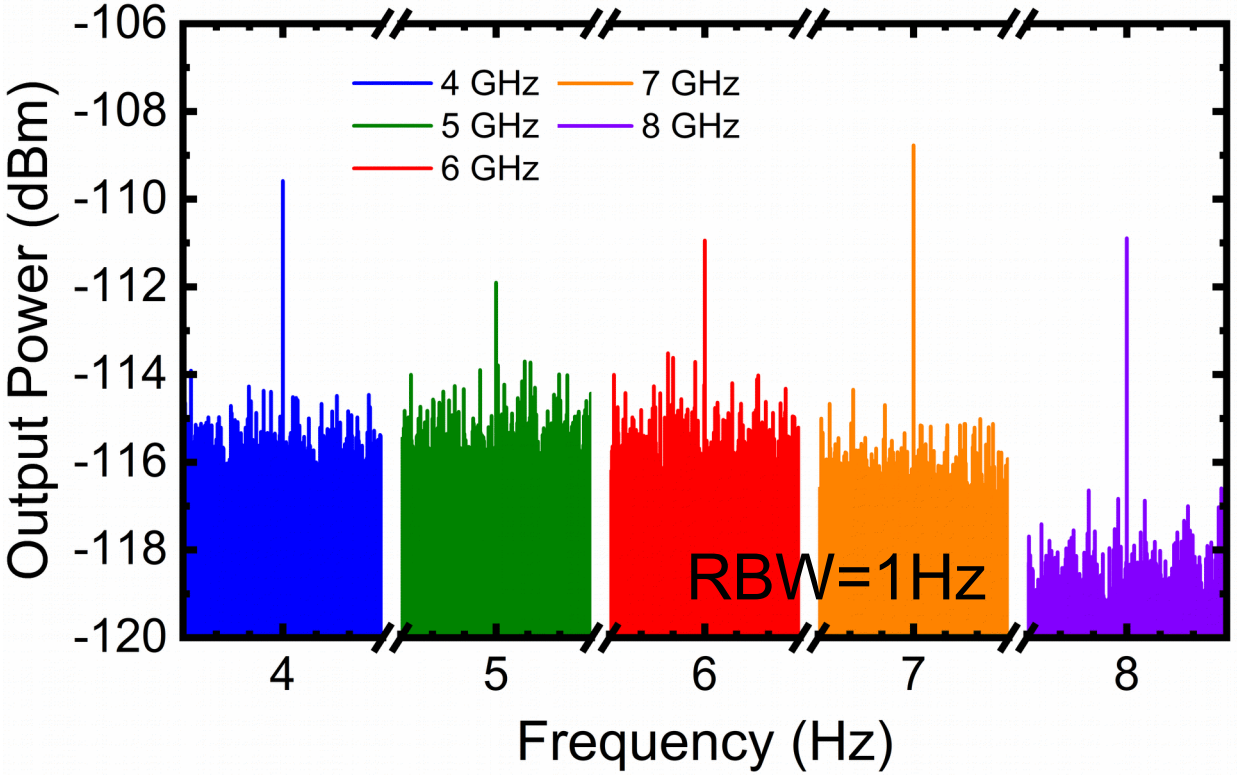
  => Z_{21} > 110 dBΩ
- Lowest possible noise
- BW > f_L /20 (f_L = 60-160 GHz)
- Z_{out} = 50 Ω
- P_{DC} < 5 mW





Meas. output spectra of 1x p-DQD+TIA at 300K





- Output spectrum measured with variable-amplitude sinusoidal signals applied to the gate of the DQD.
- At -110dBm output power, the 4GHz sinusoidal signal is clearly visible above the noise floor. Based on the 251 kΩ TIA gain, this corresponds to $3pA_{rms}$ current at the input of the TIA.

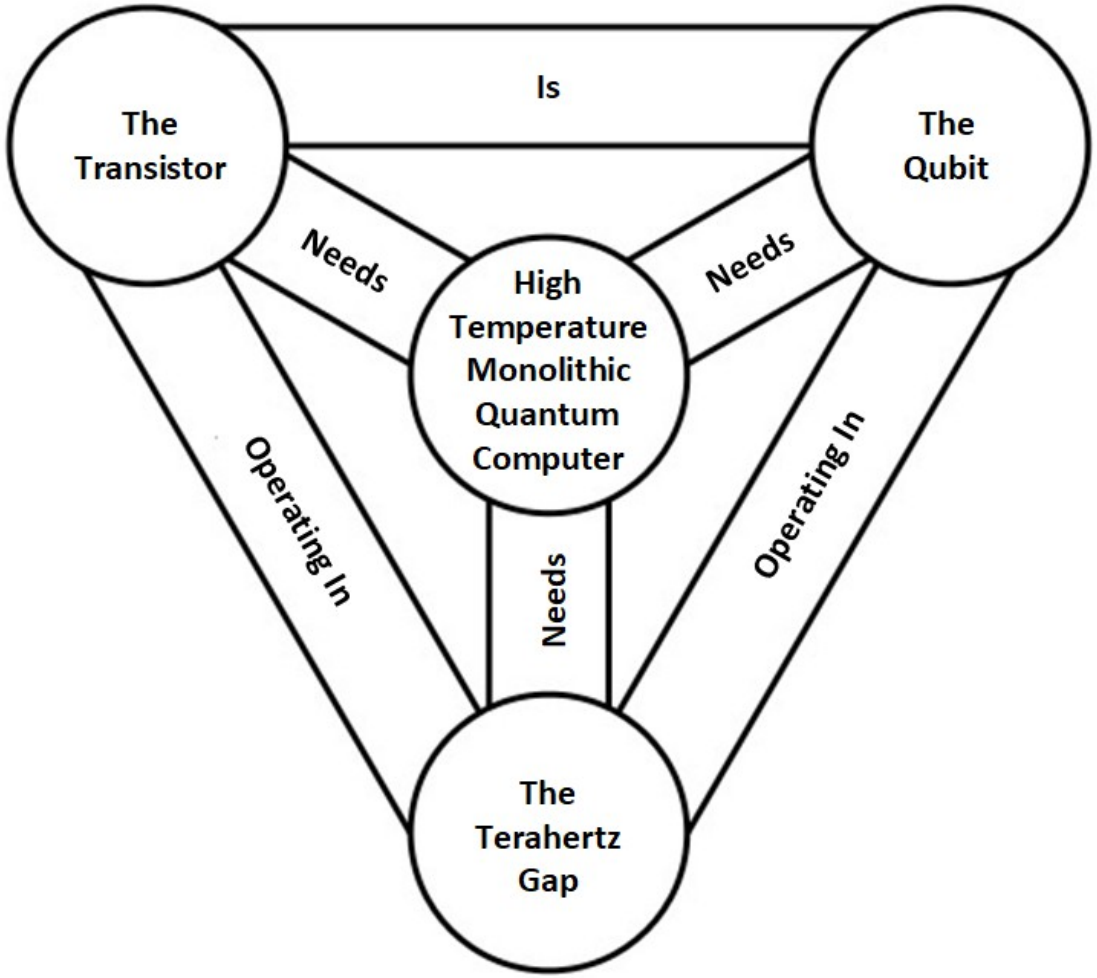
Challenges

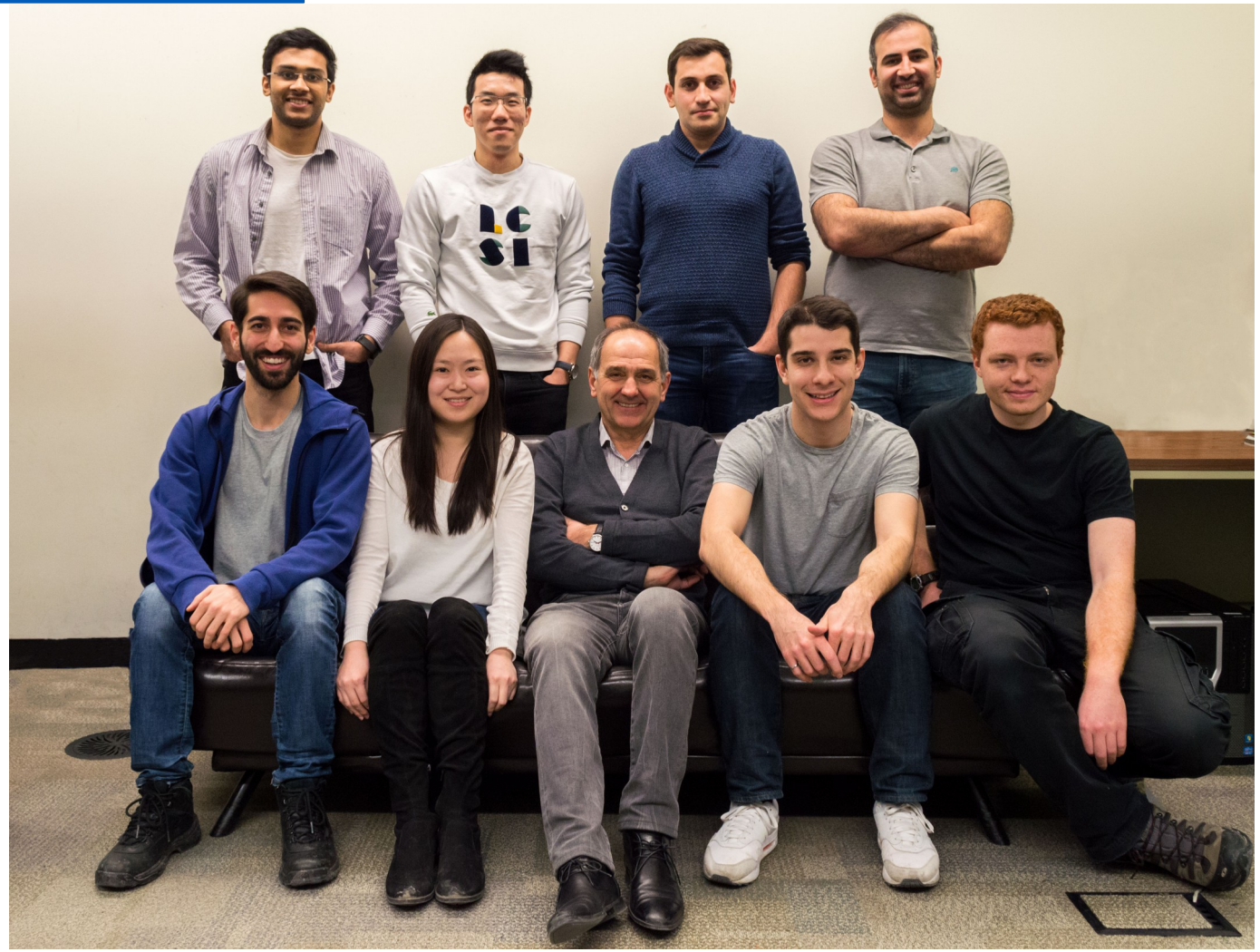
- Qubit fidelity << transistor fidelity => **Tradeoff: T vs. fidelity**
- Spin readout, qubit-to-qubit isolation
- Gyromagnetic-factor engineering for high-temp scaling
- W_f <= 50 nm (limits operation temperature today)
- CNOT Gate (or other 2 qubit logic gate)
  - (Minor) process/mask changes still needed
- Entanglement across multiple qubits

Conclusions

- **Monolithic integration** of CMOS spin control/readout circuits and qubits
- **SiGe hole-spin qubit** in p-MOSFET channel
- **> 60GHz** spin-manipulation/readout low-noise, AMS circuits needed
- At 2-4 K, minimum-size 22nm FDSOI MOSFET can be used as qubit in the subthreshold and as “classical” transistor in saturation
- 100-qubit processor < 2 W, probable now at 2-4 K in 22-nm FDSOI
- Future scaling to 10nm qubit gate length and 15nm width => 77 K operation?

In a nut shell: The Trinity





Acknowledgments

- Prof. P. Asbeck, UC San Diego
- Dr. A. Muller, Dr. M. Iordanescu, Dr. G. Adam, Dr. D. Daughton, N. Messaoudi Prof. R. Mansour, Dr. D. Harame, Dr. Nigel Cave
- Dr. D. Leipold, Dr. G. Maxim
- NSERC and EU Horizon2020 IQubits project for funding
- GlobalFoundries for technology access and chip donations
- IMT Bucharest, Lakeshore, Keysight, and U Waterloo for cryo measurements
- Integrand for EMX software
- CMC and Jaro Pristupa for CAD tools and support

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- Integrand for EMX software
- CMC and Jaro Pristupa for CAD tools and support

Multi site measurements

- IMT Bucharest: November 2017 to present
  - Custom-built cryostat DC-67 GHz, 6 K – 300 K
  - DC and non-calibrated GSG 2-port S-params w/o B-field: TIA, transistors, quantum dots, passives
- University of Waterloo, Ontario, Canada: March 2018
  - Lakeshore CPX 3.3 K commercial system
  - DC and calibrated GSG 2-port S-params: Transistors, passives
- Lake Shore Cryotronics, Westerville, Ohio, USA: June 2018)
  - Lakeshore CPX 2K commercial system
  - DC and calibrated GSG 2-port S-params: Single and double QDs, TIA

Semiconductor qubits

Information encoded in particle ***spin*** or ***charge location***

Satisfies $$i\hbar\frac{d|\psi(t)>}{dt}=\hat{H}(t)|\psi(t)>=E(t)|\psi(t)>$$

Basis states

|↑> = |0>; |↓> = |1>

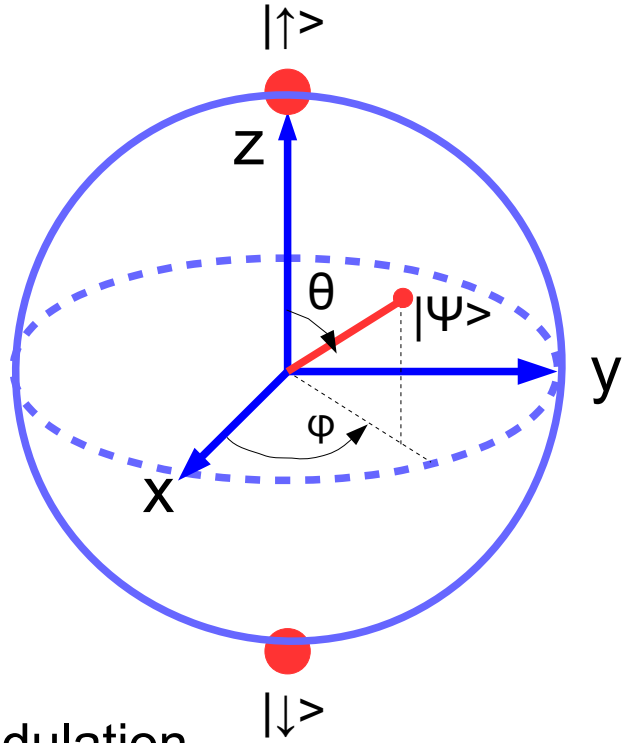
Superposition states

|Ψ> = **a**|↑> + **b**|↓>

a and **b** are ***complex*** numbers

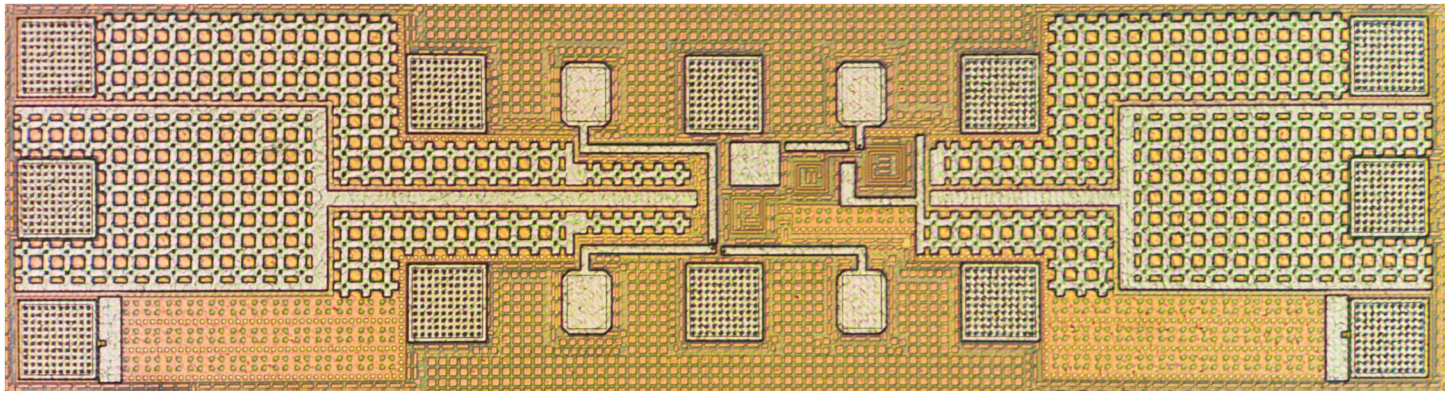
- **a** = cos(θ/2), **b** = $e^{i\varphi}$sin(θ/2)
- $|\mathbf{a}|^2 + |\mathbf{b}|^2 = 1$
- Only ***two deterministic real*** variables: φ, θ => coherent phase modulation

Bloch sphere



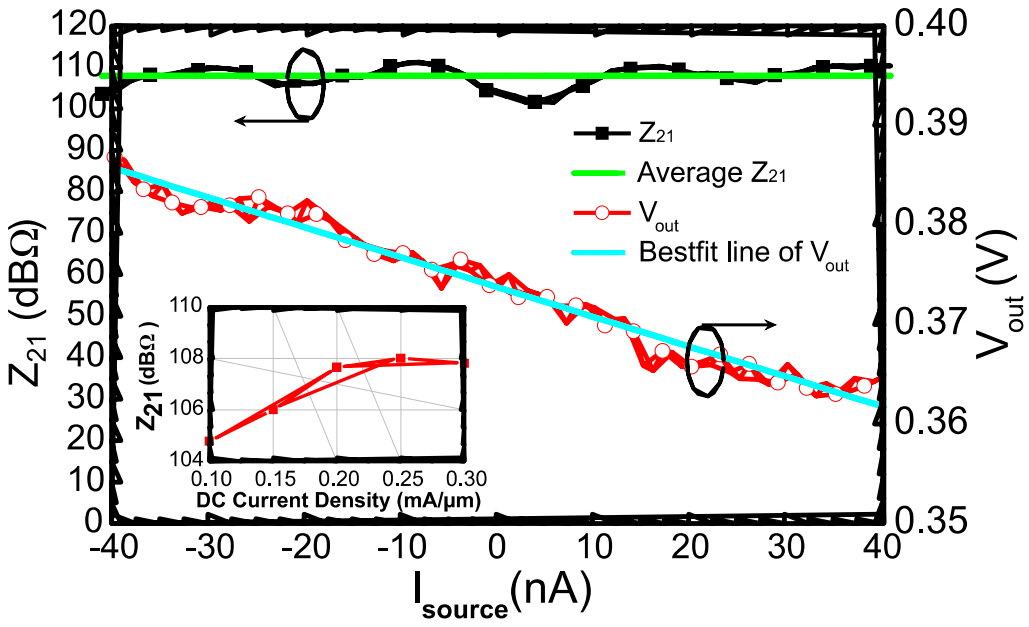
$$\tan\theta \stackrel{\text{def}}{=} \frac{\sqrt{\Delta^2+\tilde{\Delta}^2}}{\epsilon} \text{ with } 0\le\theta\le\pi \qquad \tan\phi \stackrel{\text{def}}{=} \frac{\tilde{\Delta}}{\Delta} \text{ with } 0\le\phi\le 2\pi$$

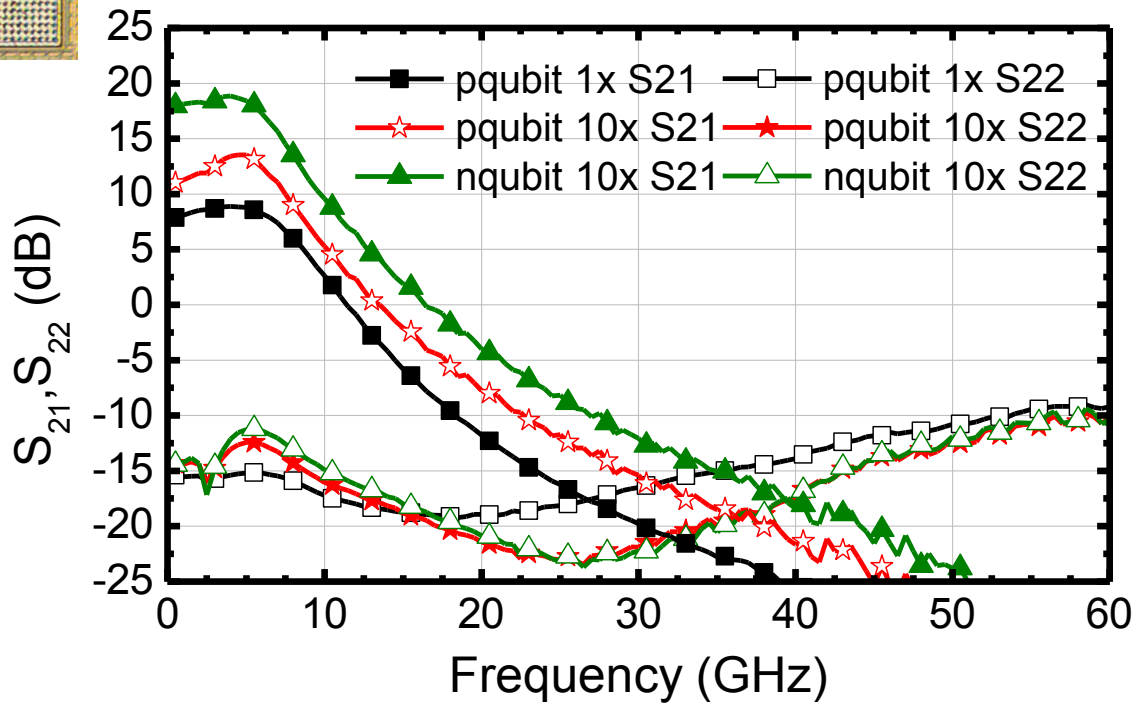
10 coupled double QD qubits with TIA readout



Improved gain and bandwidth

[M. Gong et al. RFIC 2019]





SiGe HBT performance improves at 6-80 K

0.1x4.5µm CBEBC