Testing Requirements for Emerging Single-Chip Cryogenic Mixed-Signal Quantum Processors in Production 22nm FDSOI CMOS Technology

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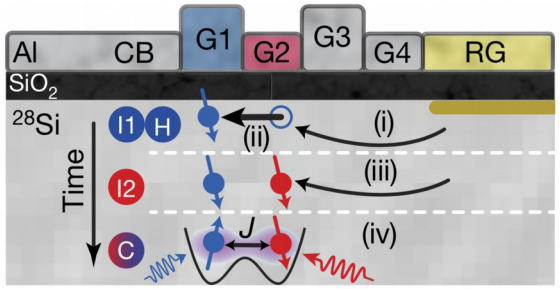
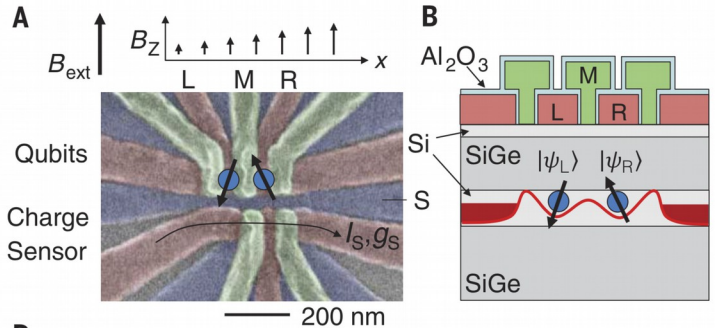
Outline

- *Introduction*
- Qubit and Processor Testing Considerations
- Cryogenic Technology Measurements
- Conclusions

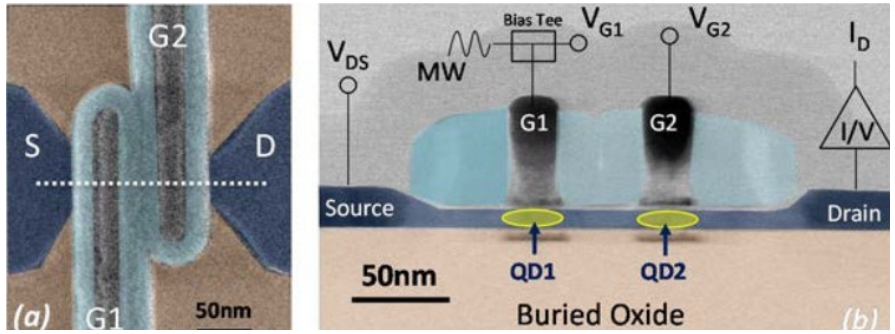
Semiconductor Quantum Dot (QD) qubits



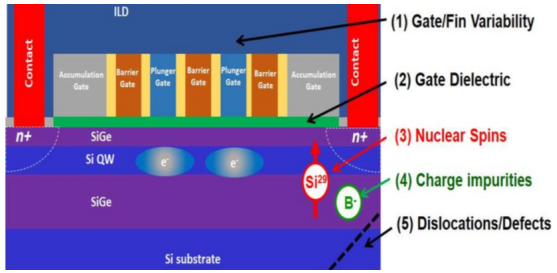
[W.Huang, Nature 2019]

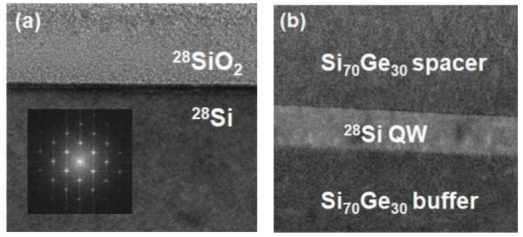


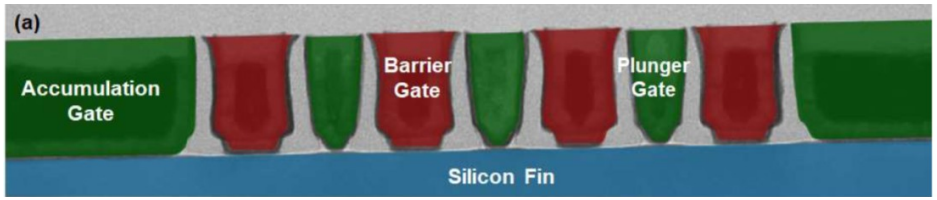
[D.M. Zajec, Science 2018]



[L. Hutin, VLSI 2016]







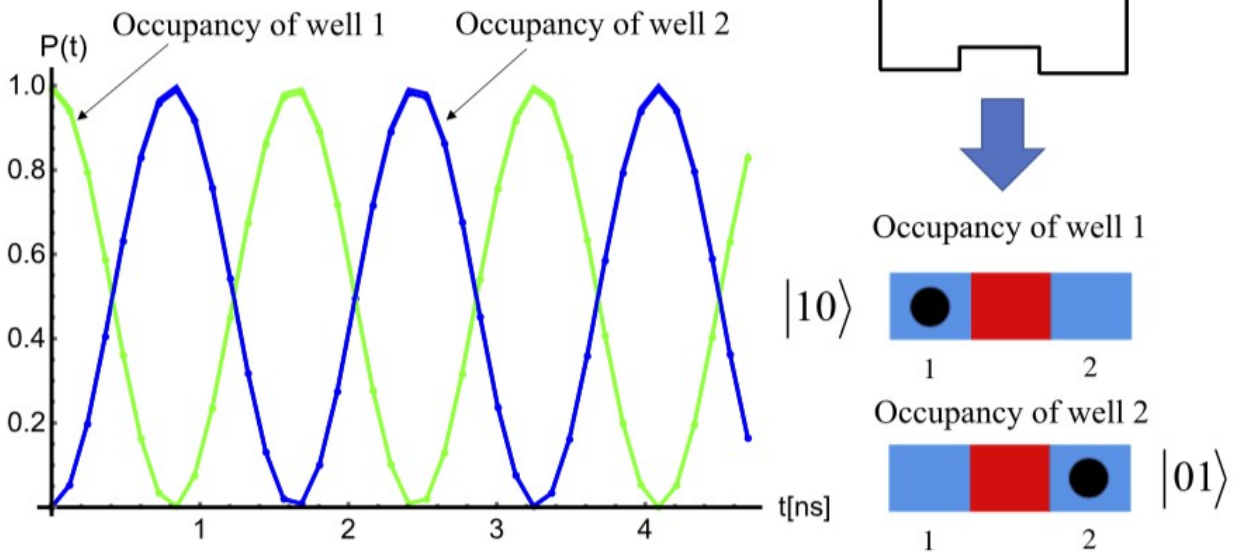
[Intel, IEDM 2018]

- Qubits formed in QDs where electrons/holes are confined by an energy potential well created in the conduction/valence band of a semiconductor structure: Si, Si/SiGe MOSFET, FDSOI, FinFET
- QDs placed in close proximity to enable tunnel coupling, a function of barrier height/thickness
- Two adjacent (usually lowest) energy levels in QD used to create basis states |0> and |1>

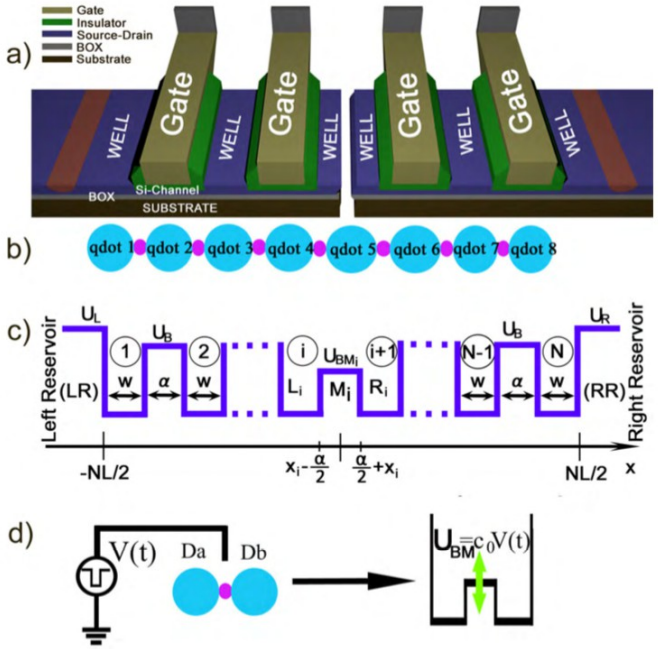
Charge qubit concept in FDSOI

- Similar to charge coupled devices
- Gates control barriers (tunnel coupling, ***t***) between QDs
- Degree of freedom is position of electron in DQD
- Voltage applied between dots creates detuning: $E_{P1} \neq E_{P2}$
- Rabi frequency, f_R, from probability oscillation

$$f_R = \frac{2t}{2\pi\hbar}$$



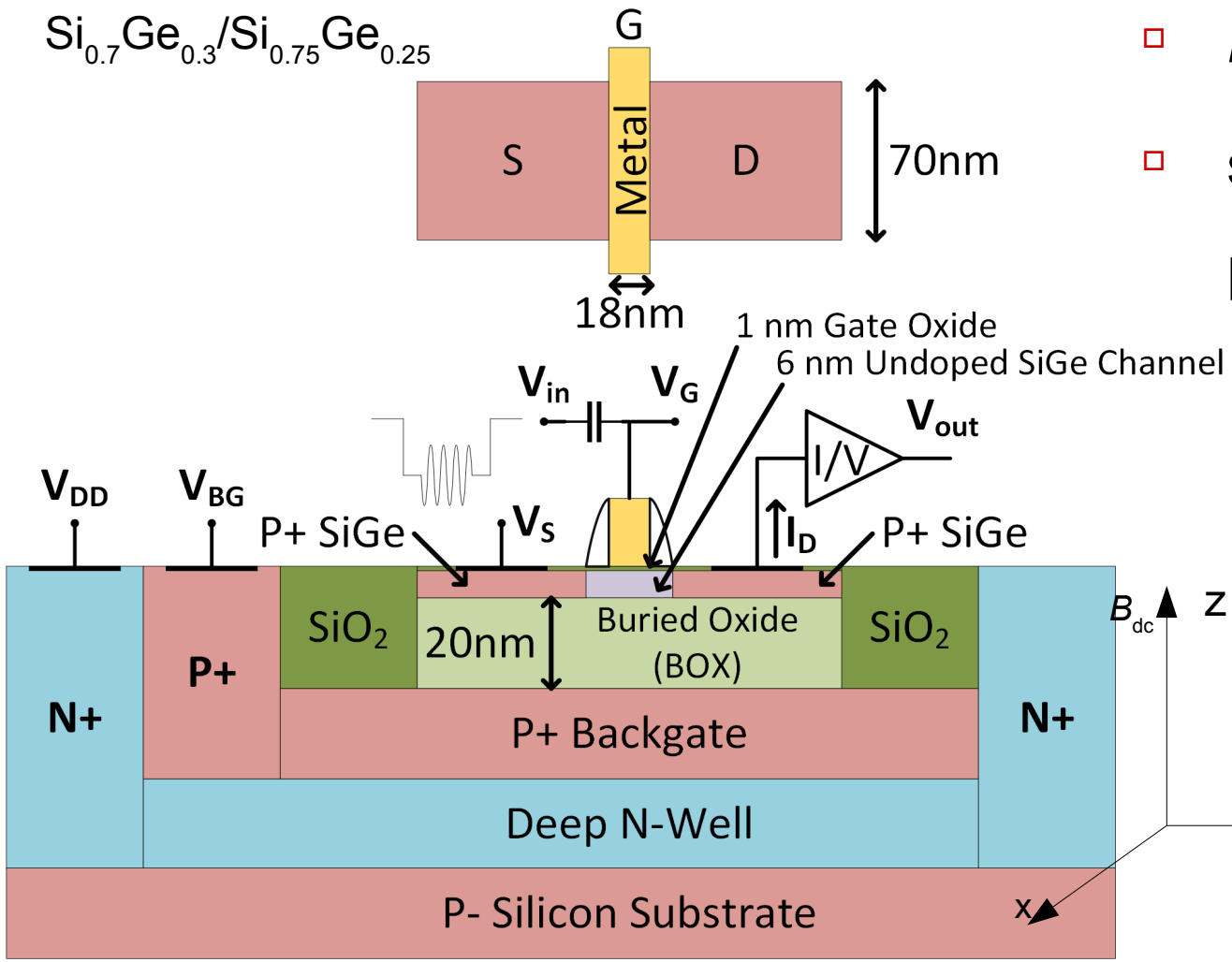
[P. Giounanlis et al. 2019]



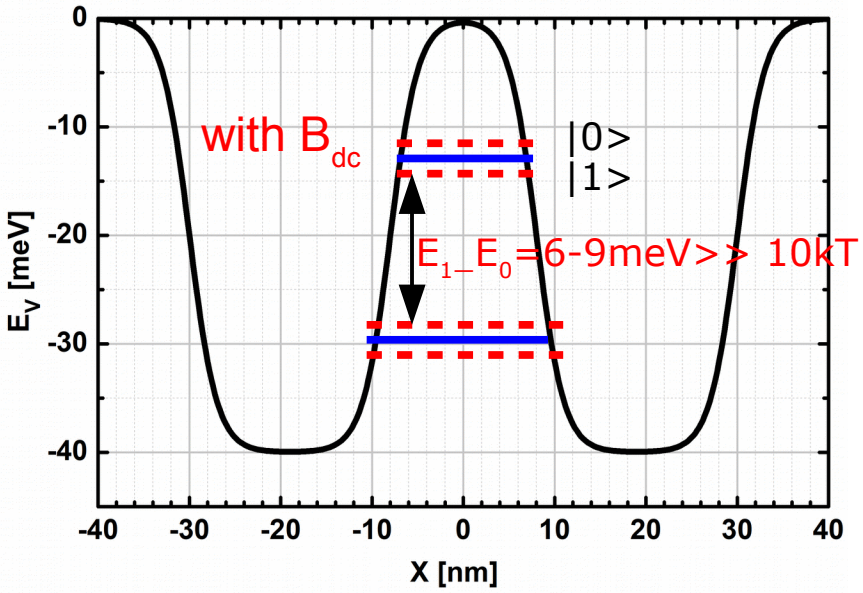
$$\hat{H} = \begin{bmatrix} E_{P1} & t \\ t & E_{P2} \end{bmatrix}$$

$$|\psi(t)> = a(t)|10> + b(t)|01>$$

Hole-spin qubit concept in FDSOI

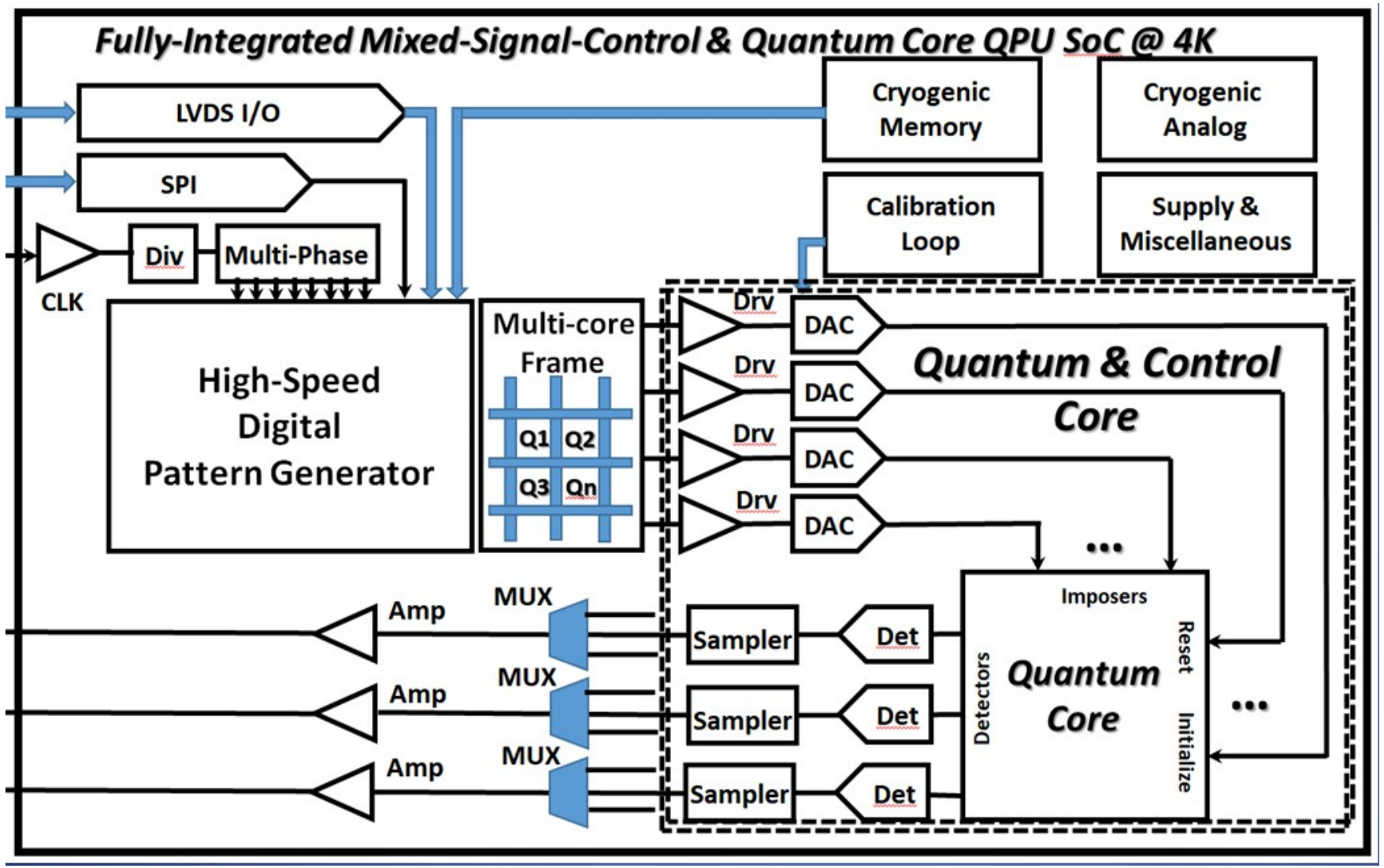


- L=18 nm; W = 50 nm
- source/drain-to-channel heterojunction: ΔE_V = 35-40 meV



[S. Bonen, et al. 2019]

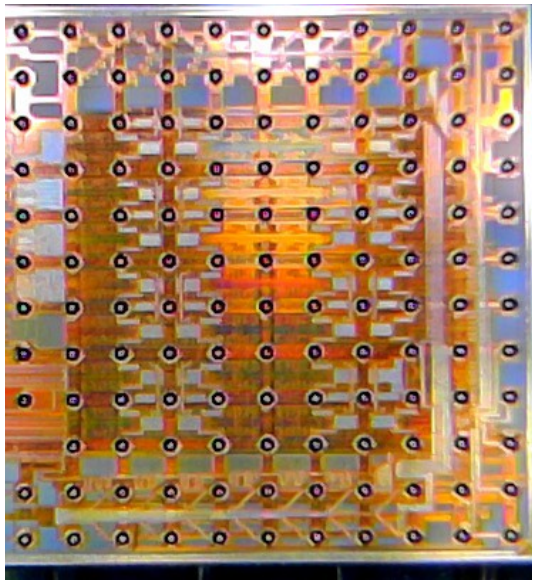
Equal1.lab 22nm FDSOI QPU for 4K operation



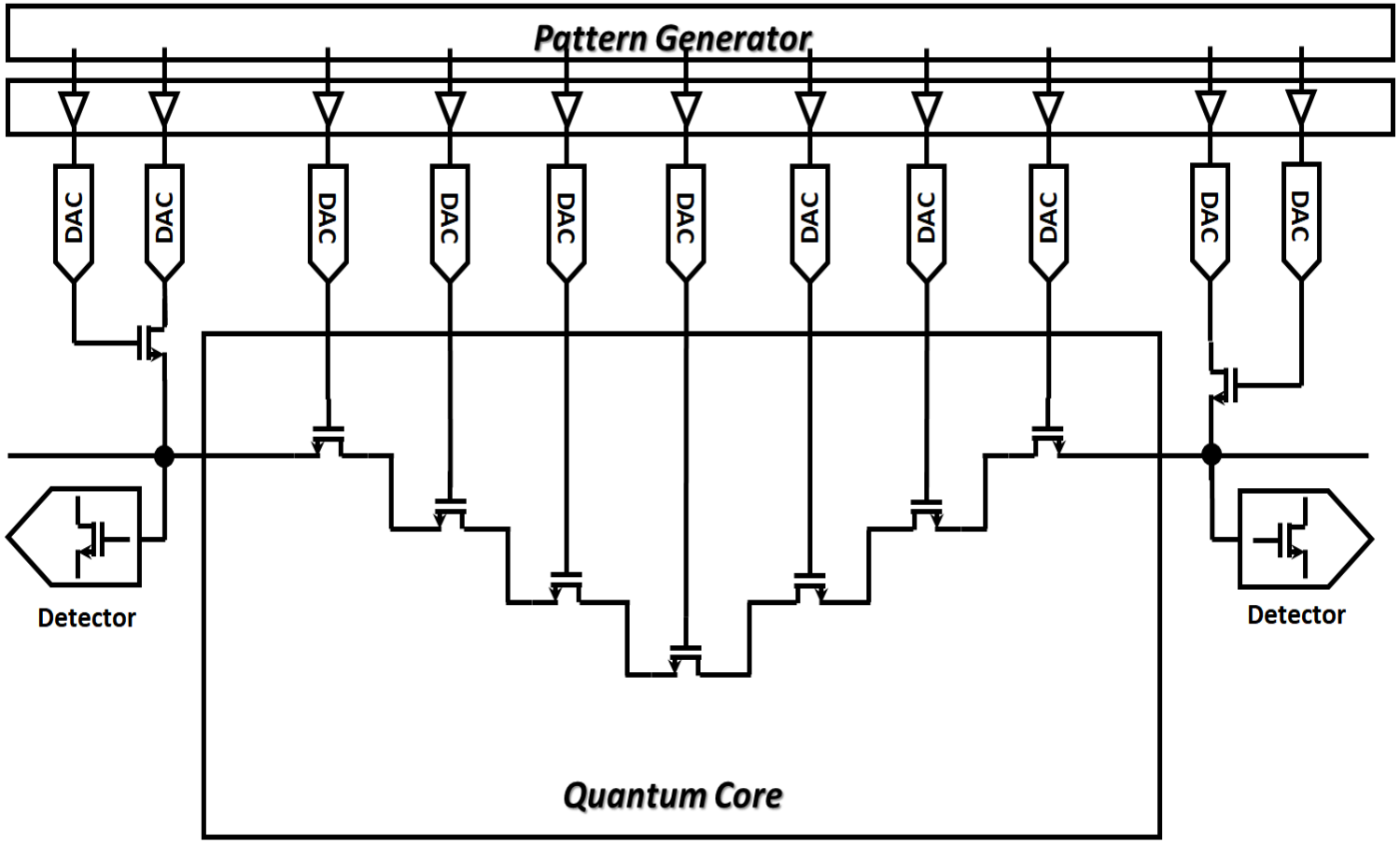
[D. Leipold, et al. 2019]

Fully-integrated SoC

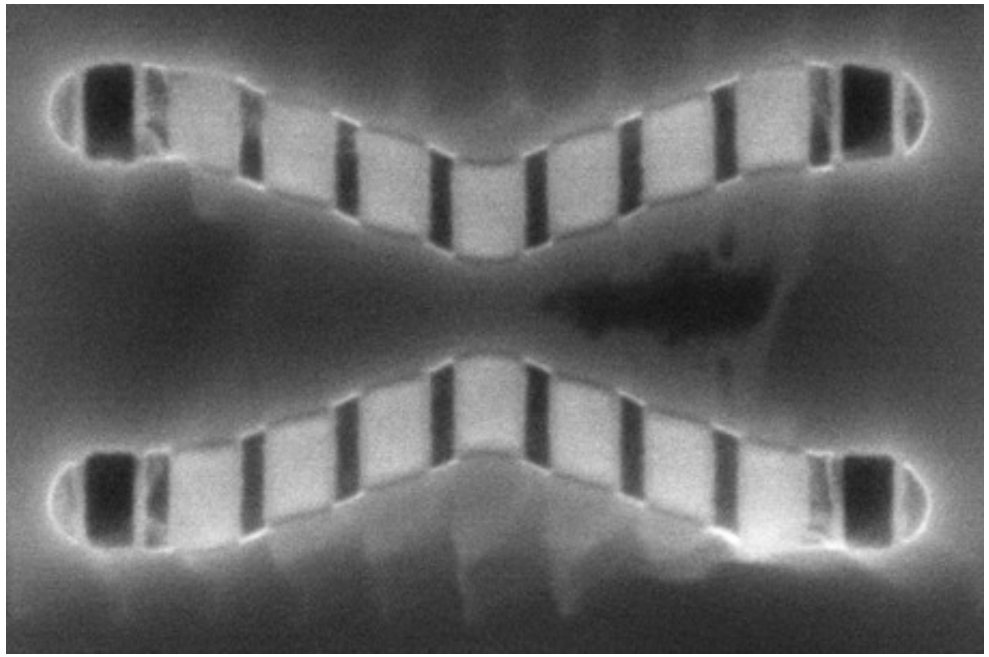
- **Quantum**
- **Analog**
- **Mixed-signal**
- **Digital**



Equal1 Quantum Core: charge qubit array



2D structure allows Topological quantum computer



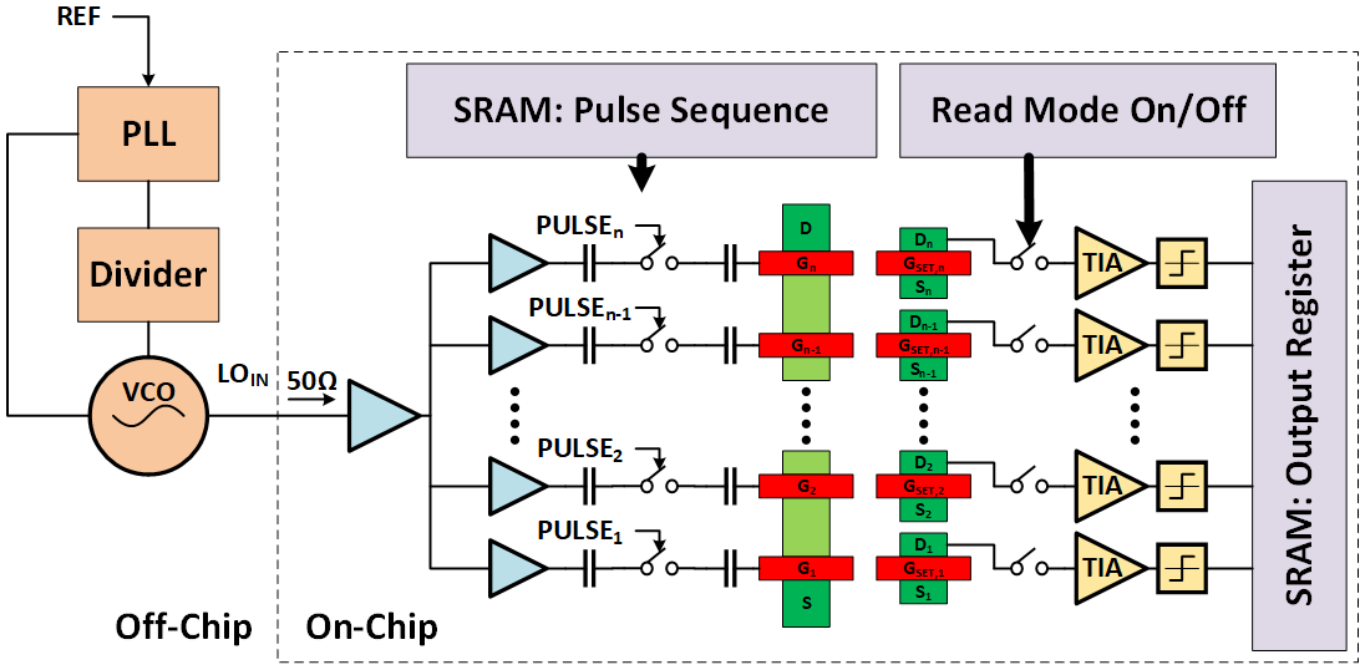
Patented quantum structures In customized GlobalFoundries FDX process

Quantum structure & tightly integrated control & interface

[D. Leipold, et al. 2019]

Hole-spin mm-wave QPU for 3-12K operation

- **Qubit array**
  - 5 pW (100pA/50mV) per qubit
  - 10^{10} qubits = 50 mW
- **Spin manipulation**
  - low phase noise (OFDM) signal at
  - 60-100 GHz for 3-5 K operation
  - 140-240 GHz for 8-12 K operation
  - n-MOSFET switch+phase pulse modulators



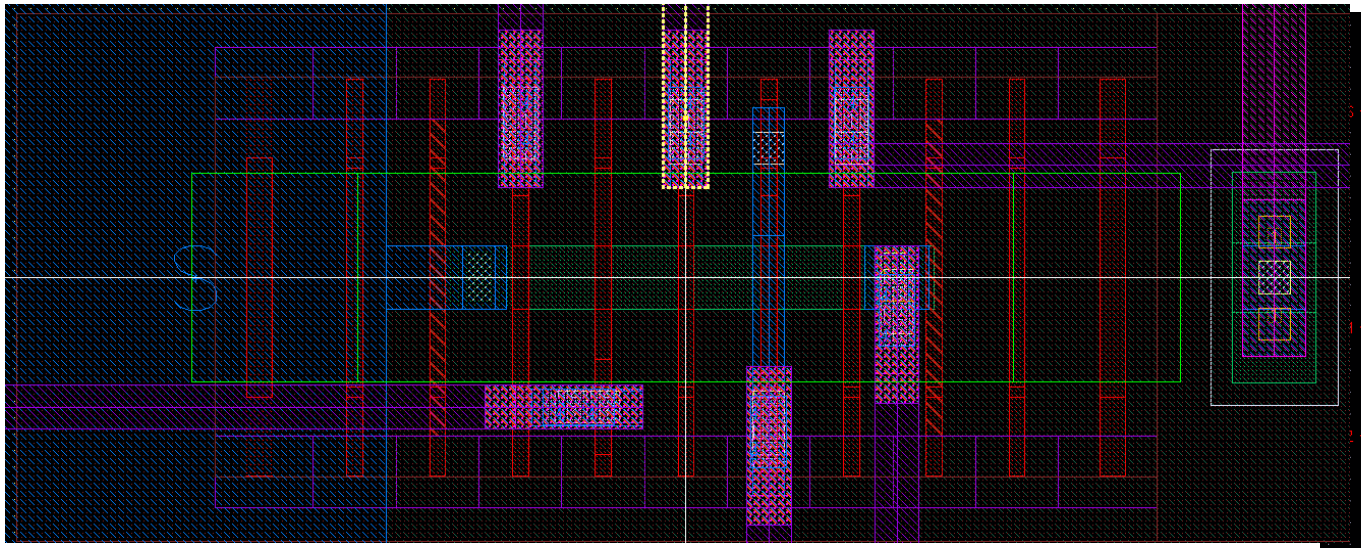
Note: qubit bias scheme not shown

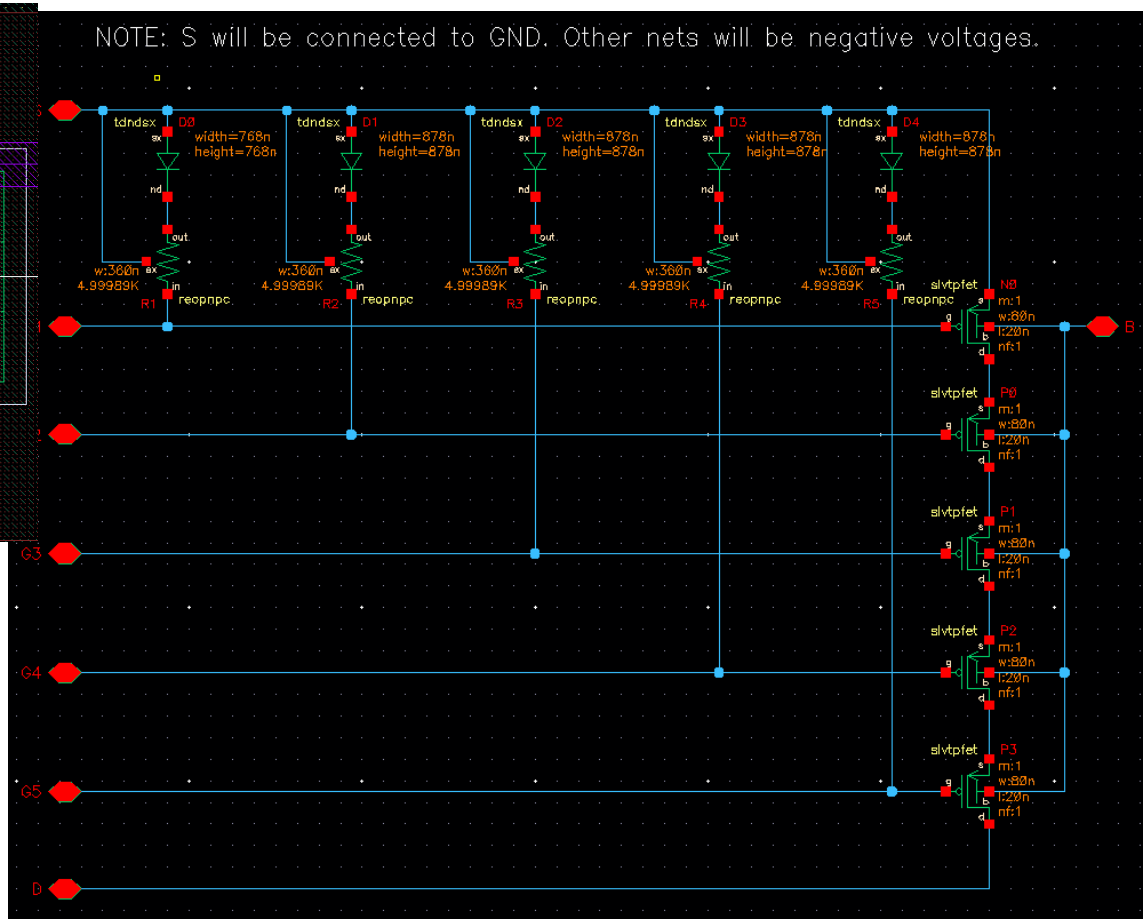
$$P_{dc}=0\,; \qquad P=\frac{f_R}{2}C\cdot V_{DD}{}^2$$

- **SRAM** stores digital pulse sequences (gate operations)

Control/readout circuits dominate consumption. Integration limited by **cryostat lift**

5 coupled quantum-dot hole-spin qubit array





- 5 gates = 5 serially coupled qubits
- similar to CCDs and stacked cascodes
- Antenna diodes included

[S.Bonen et al. EDL 2019]

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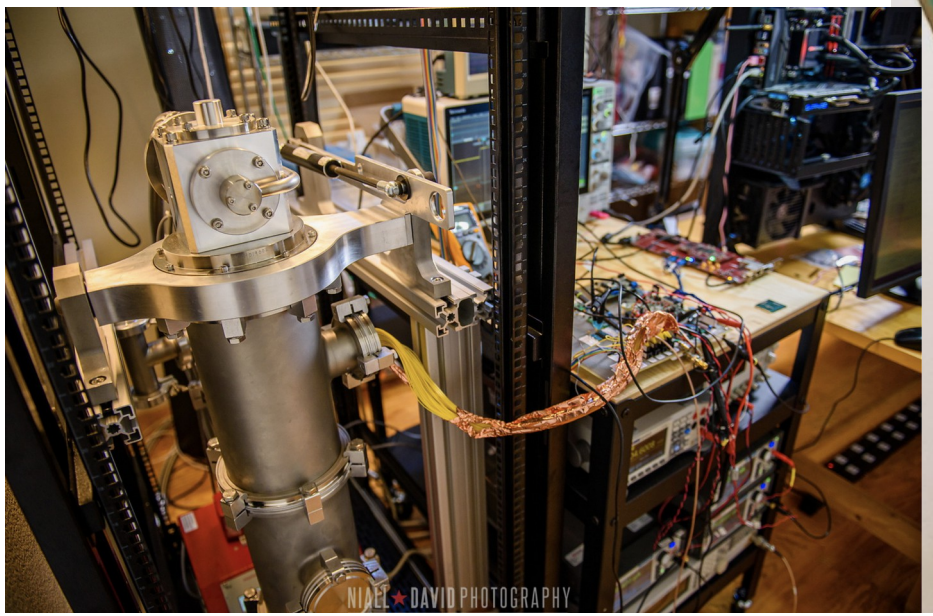
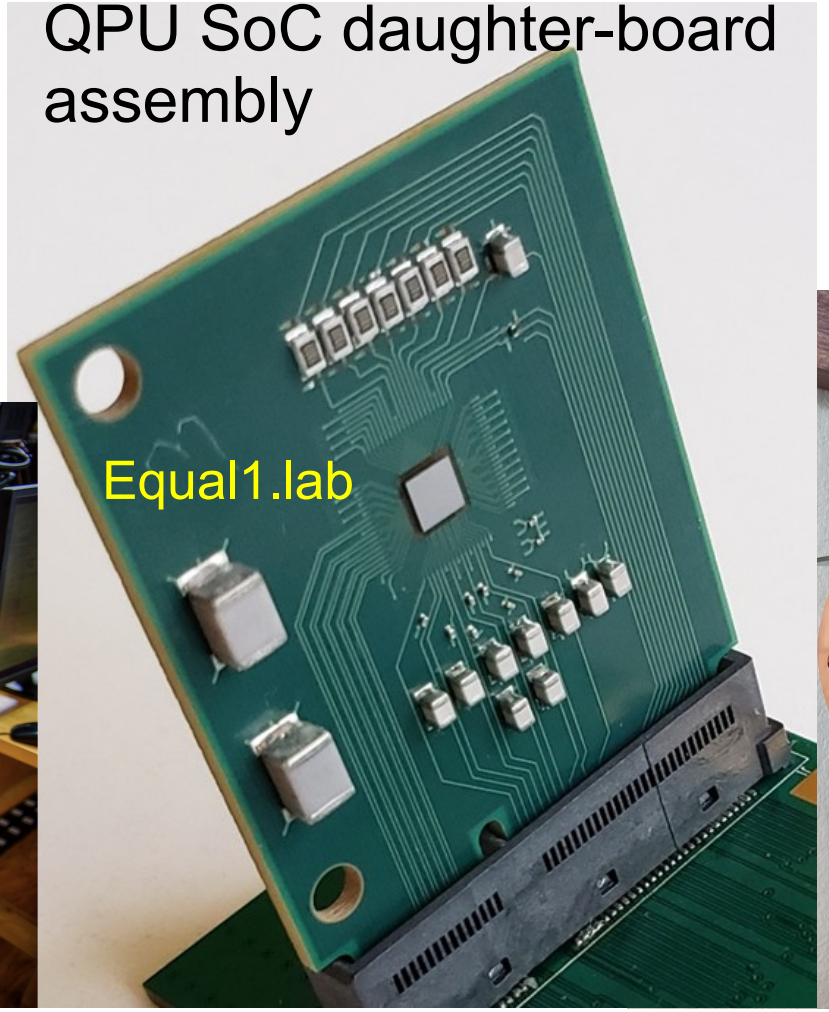
Charge QPU with built-in self-test in cryostat

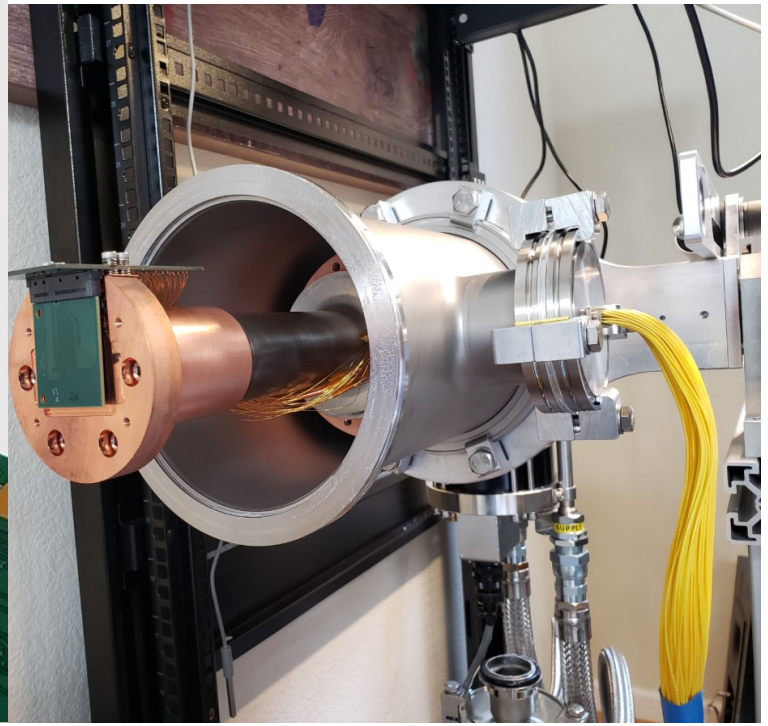
- Cryo-packaging solution
- Cable thermalization
- Impact of circuitry on qubit testing difficult to separate



QPU SoC daughter-board assembly

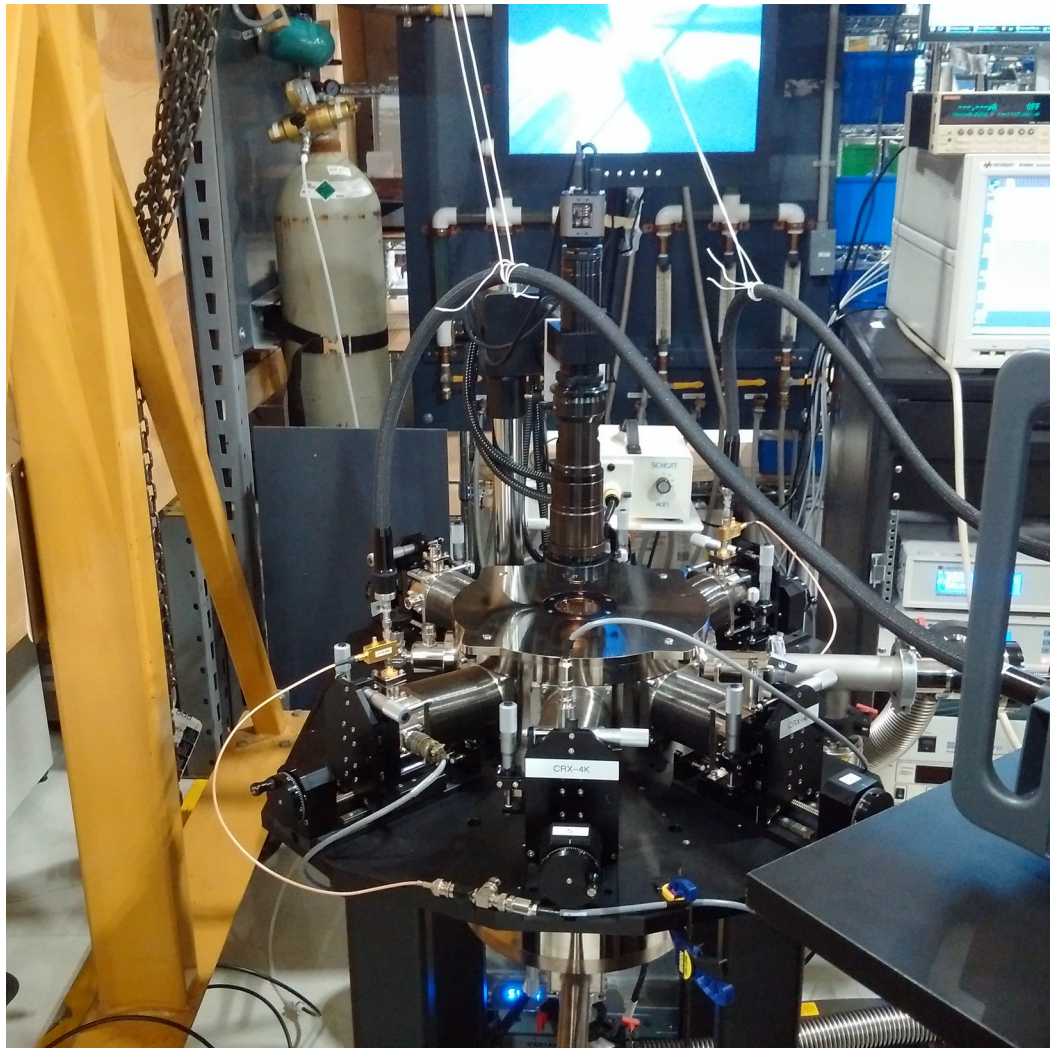


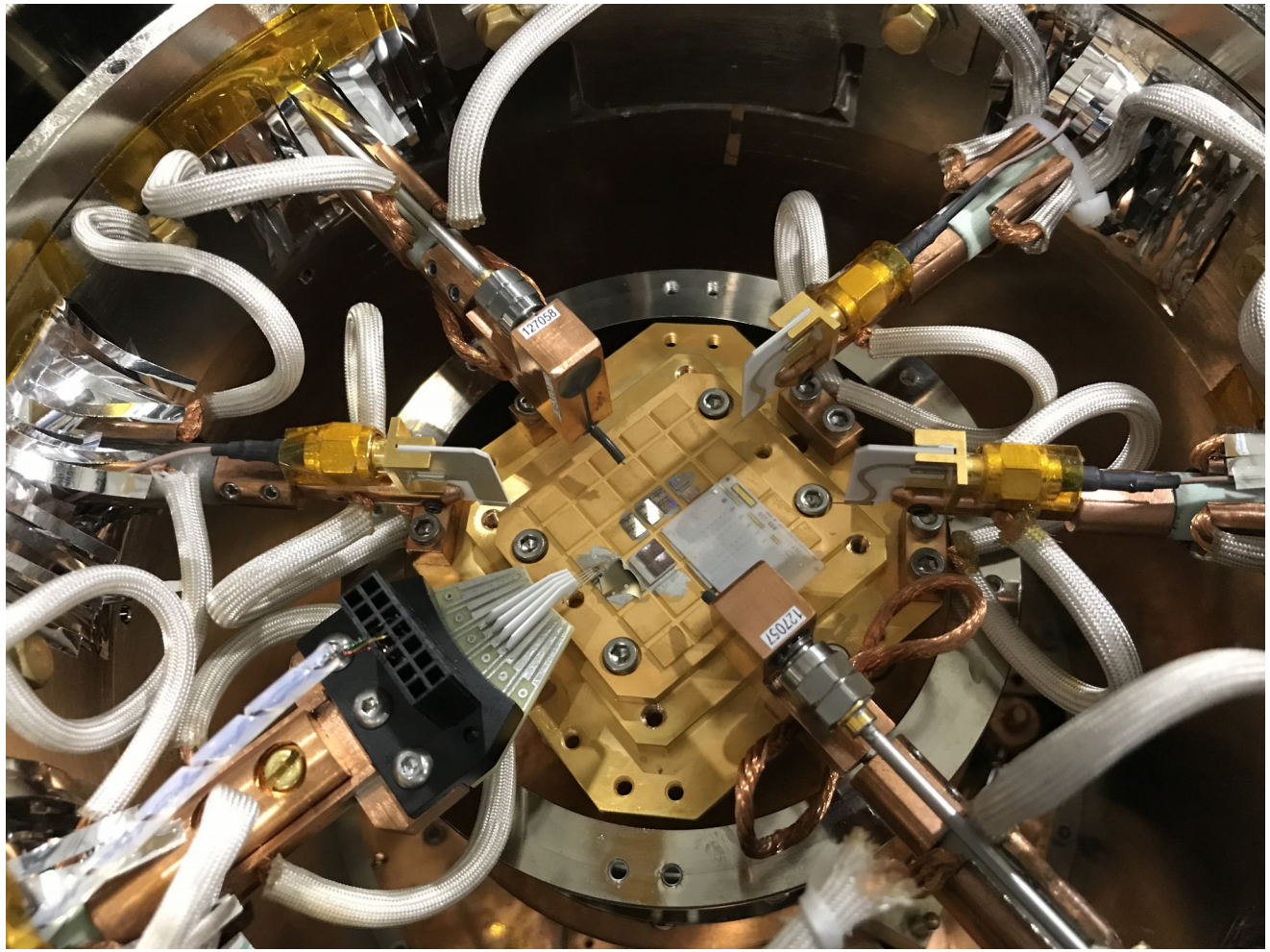
Cryo-Finger Assembly



[D. Leipold, et al. 2019]

Mm-wave cryogenic die probing





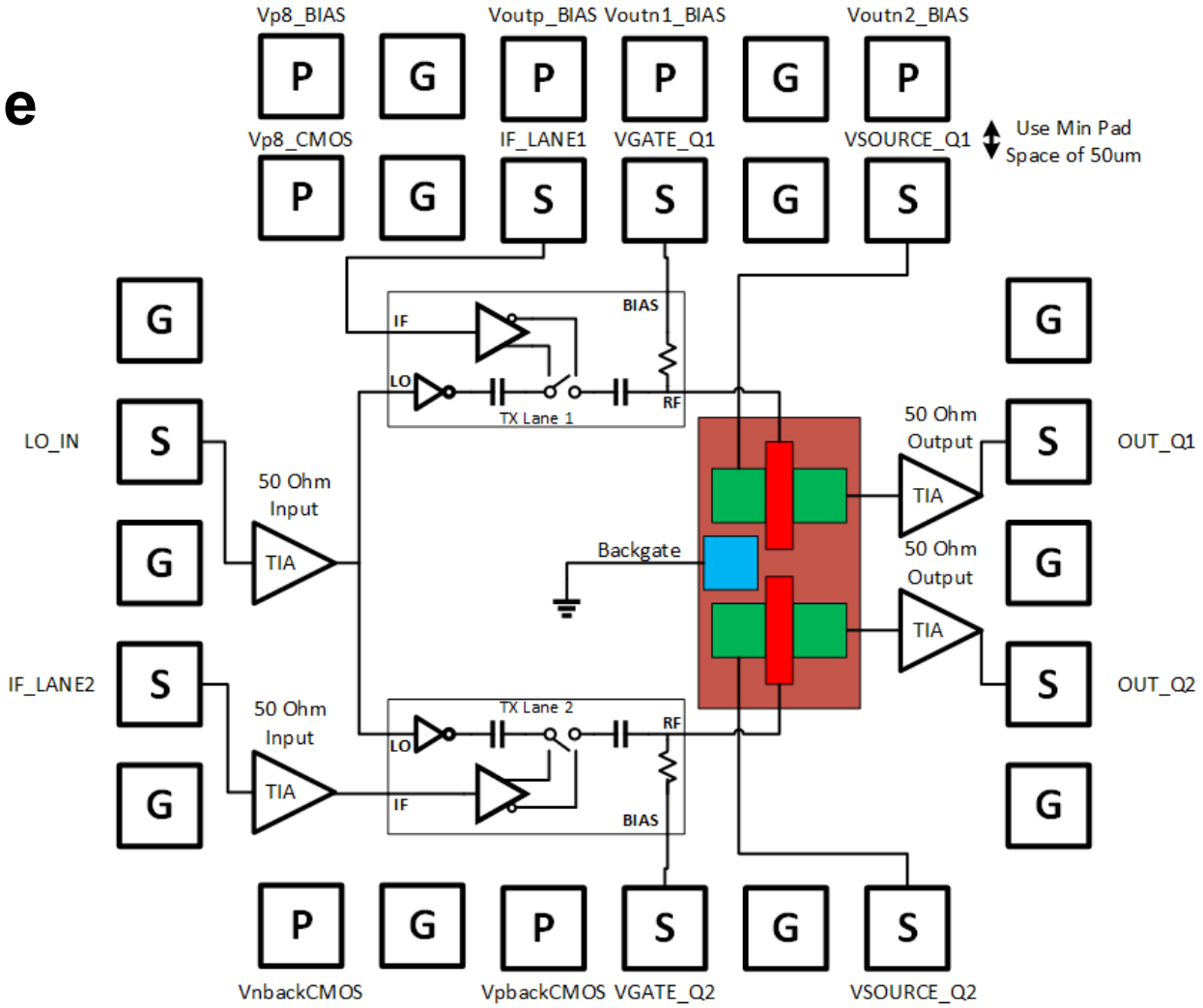
On-die cryogenic test challenges

Define common transistor, passives, SET, DQD, circuits, processor padframe

Padframe and complexity of probes, circuits, processor limited by cryostat DC power lift

Measurements limited to

- **2 Kelvin – 300 Kelvin**
- **dc-67 GHz and 140-220 GHz,**
- **B < 2.5 Tesla**
- **P_{DC} < 30 mW**



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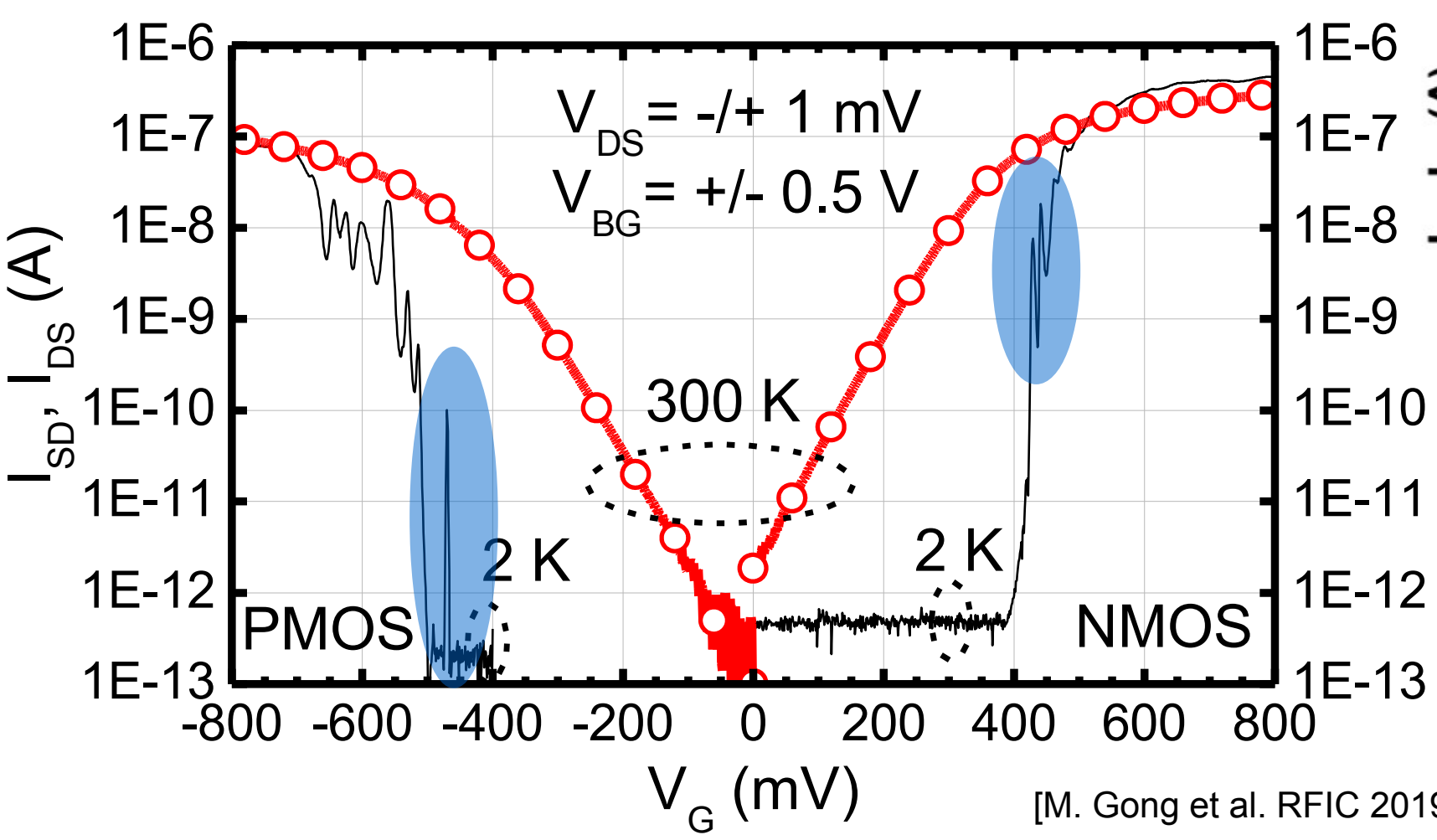
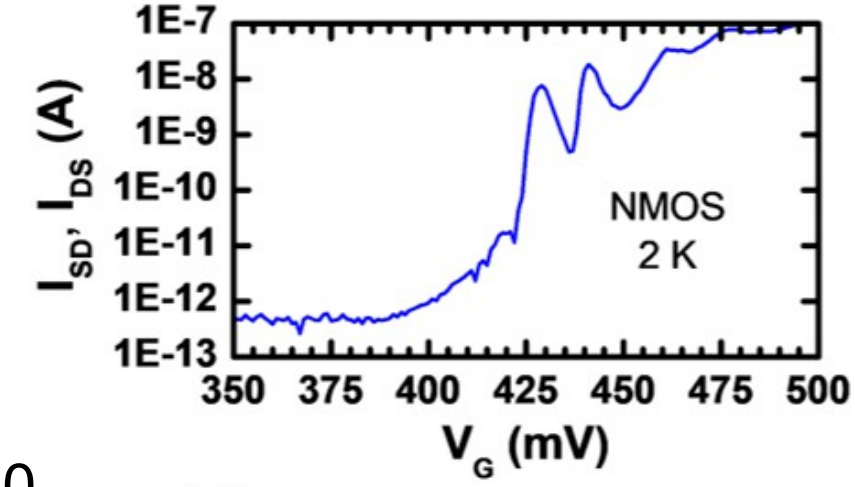
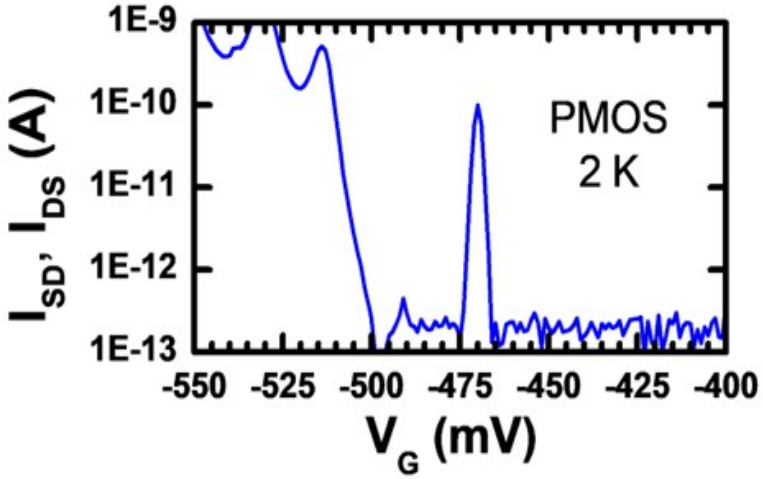
Minimum-size 20nmx80nm MOSFETs: quantum behaviour at low V_{DS} and 2 K

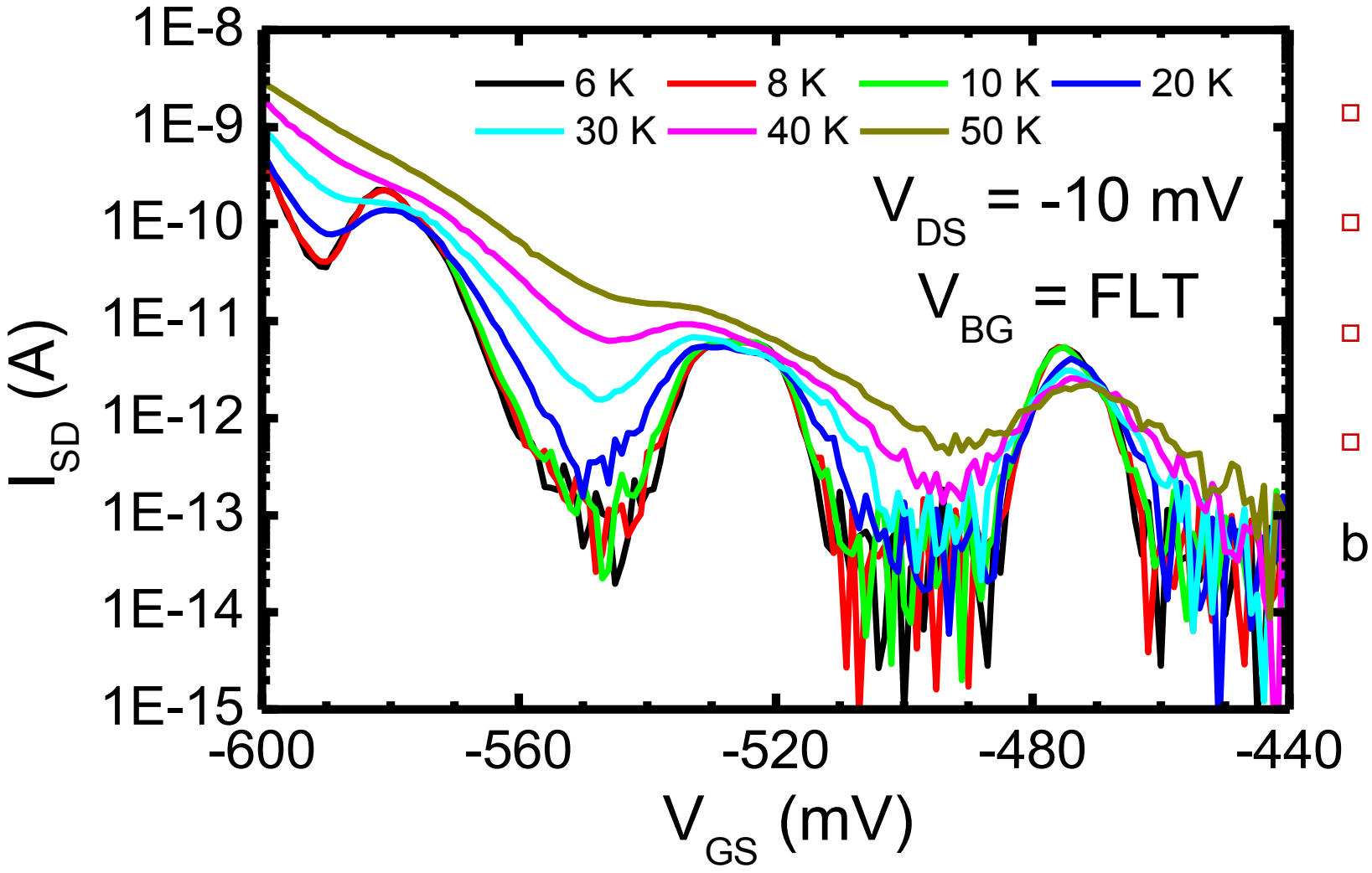






[M. Gong et al. RFIC 2019]

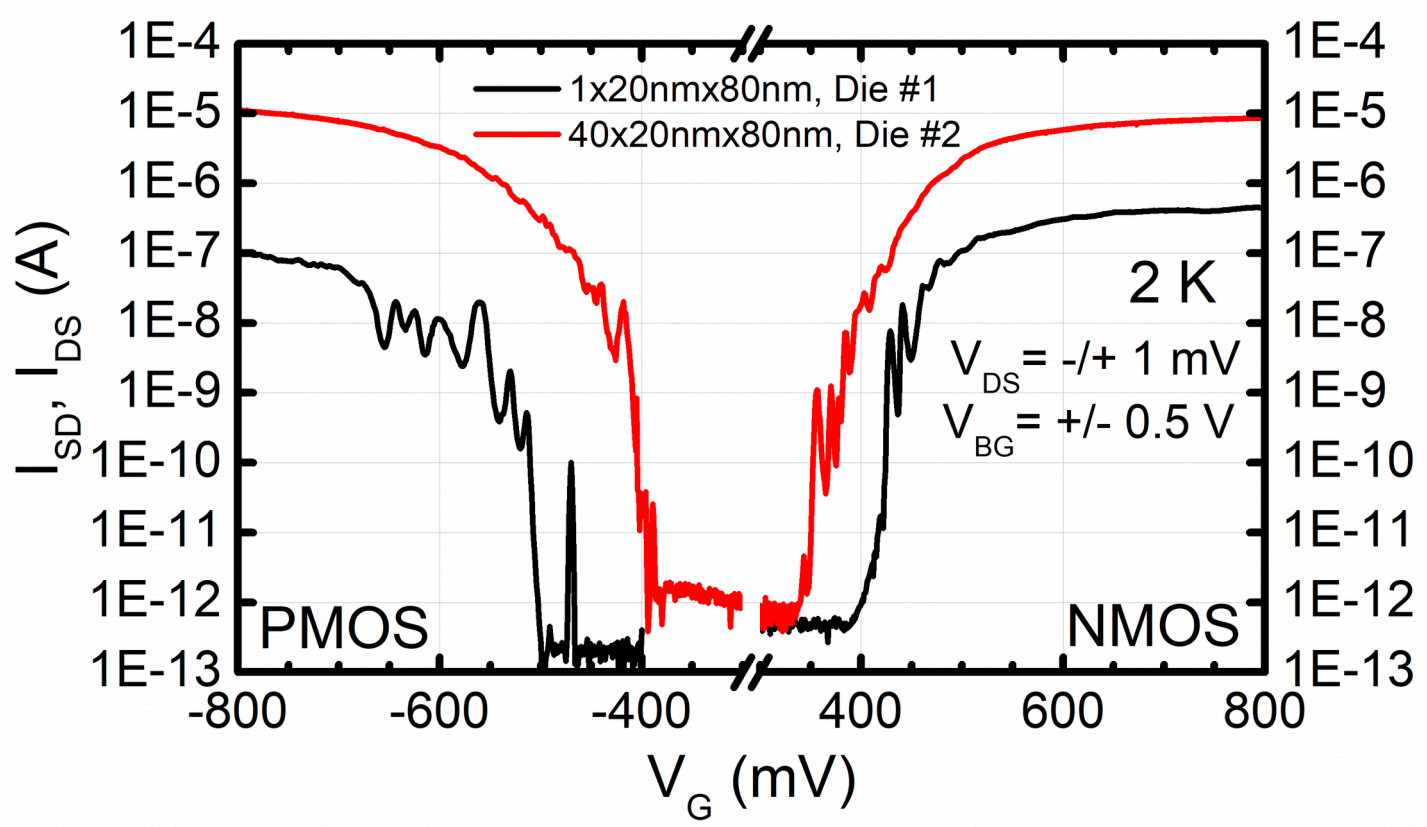
Quantum behaviour of 18nmx70nm p-MOSFET beyond 20 K



- 50-60 mV between peaks
- 5-10 pA current peaks
- peaks flatten as T increases
- qubit manipulation when biased at first valley

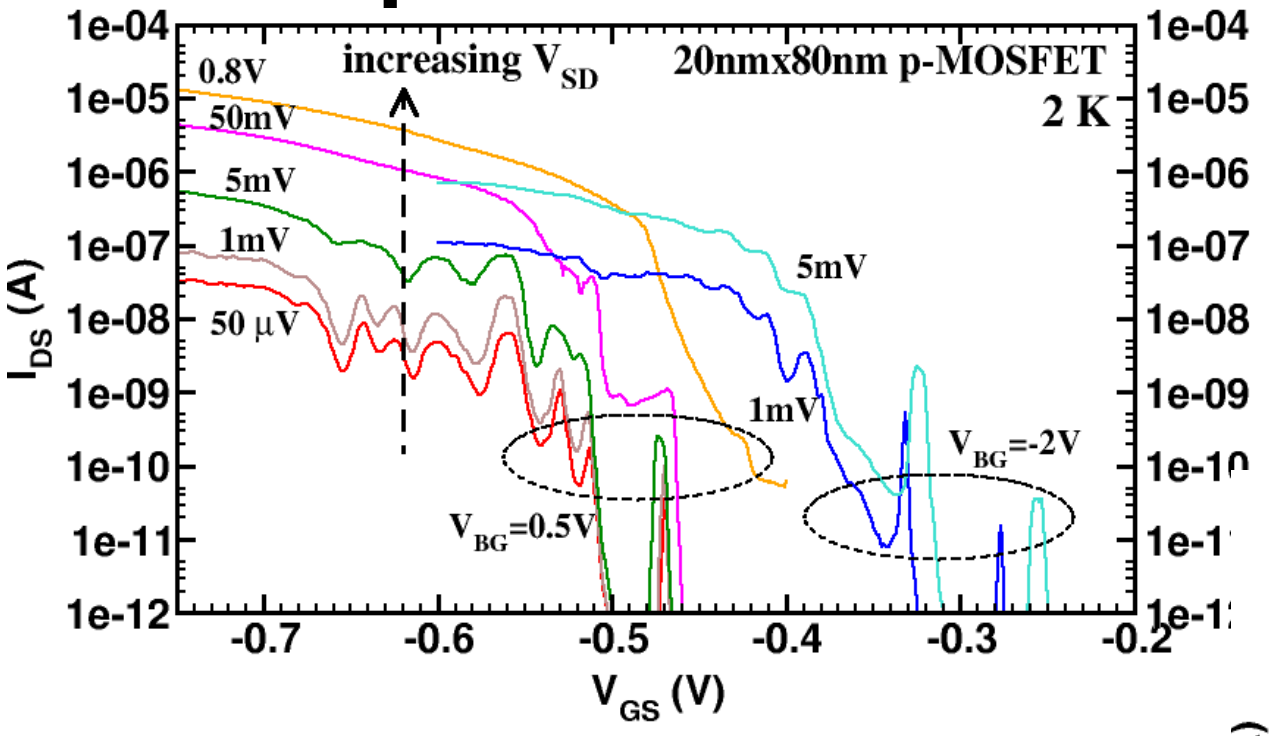
Process variation: die to die and different N_f

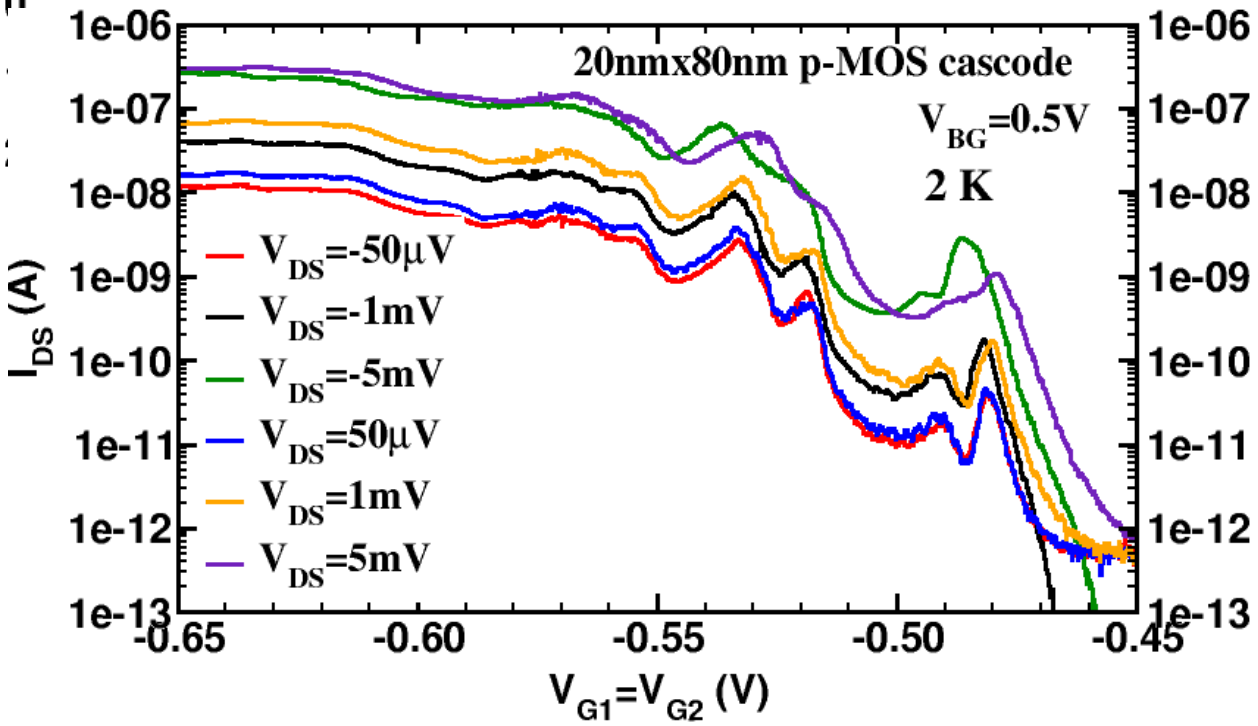
- ΔW, ΔL, $\Delta t_{Si(Ge)}$ => E_1-E_0, f_R
- Gate oxide spacer and source/drain-to-channel potential barrier => E_1-E_0
- Surface roughness => E_1-E_0
- Δt_{OX}, ΔW, ΔL, $\Delta t_{Si(Ge)}$ => V_t, f_R variation
- g?, f_{Larmor}, f_R



Some of them may be adjustable/corrected from back gate

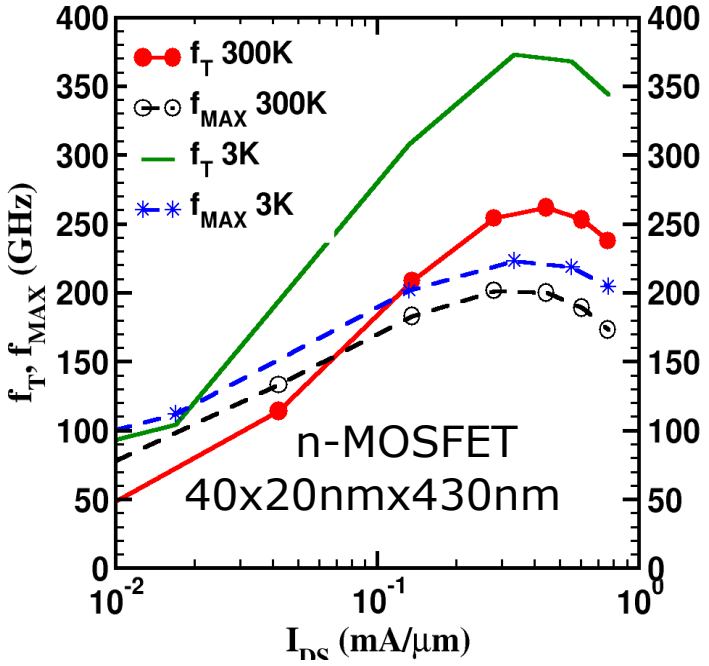
Less process variation in quantum dot arrays

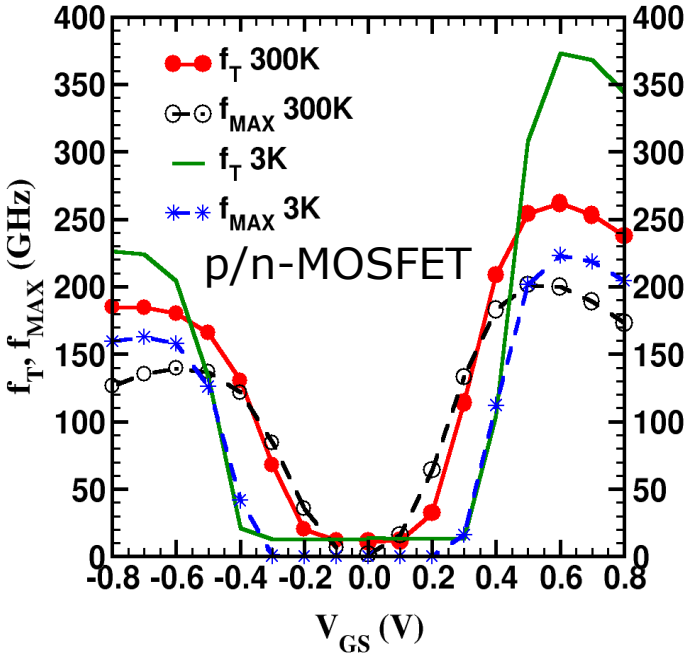


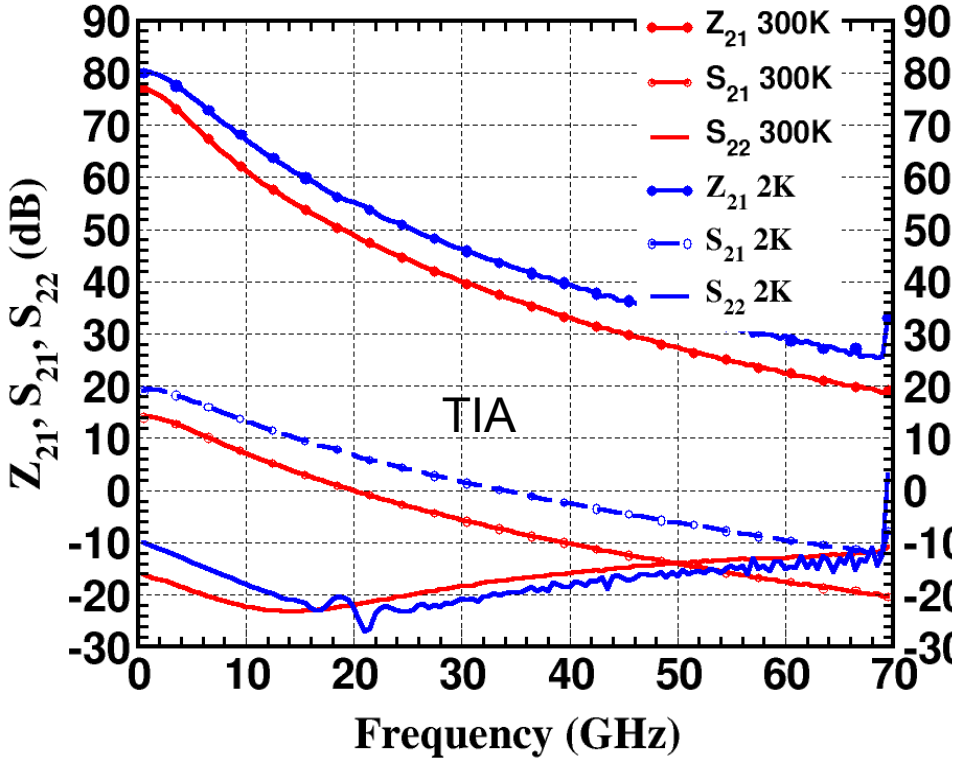


- First MOSFET peak at V_{GS} = -475 mV
- First cascode peak at V_{GS} = -480 mV
- V_{GS} of peak tuneable from V_{BG}

HF performance improves at 2-3 K



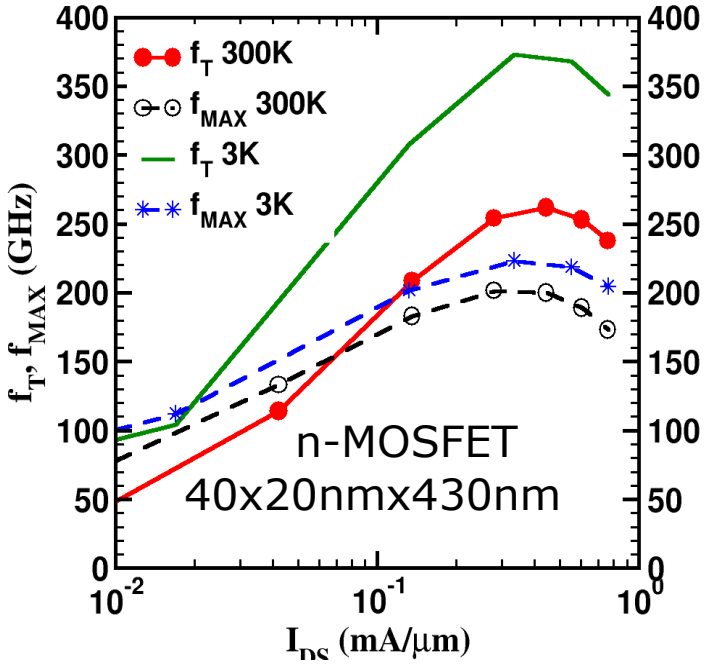


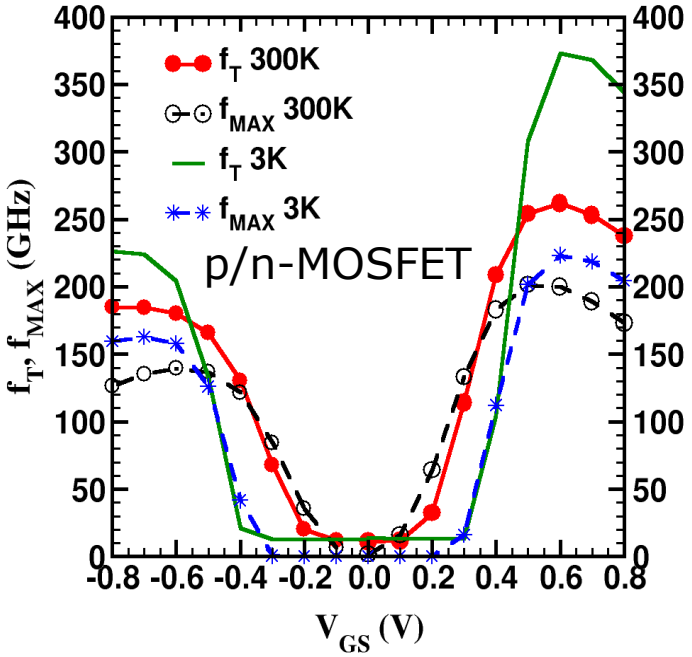


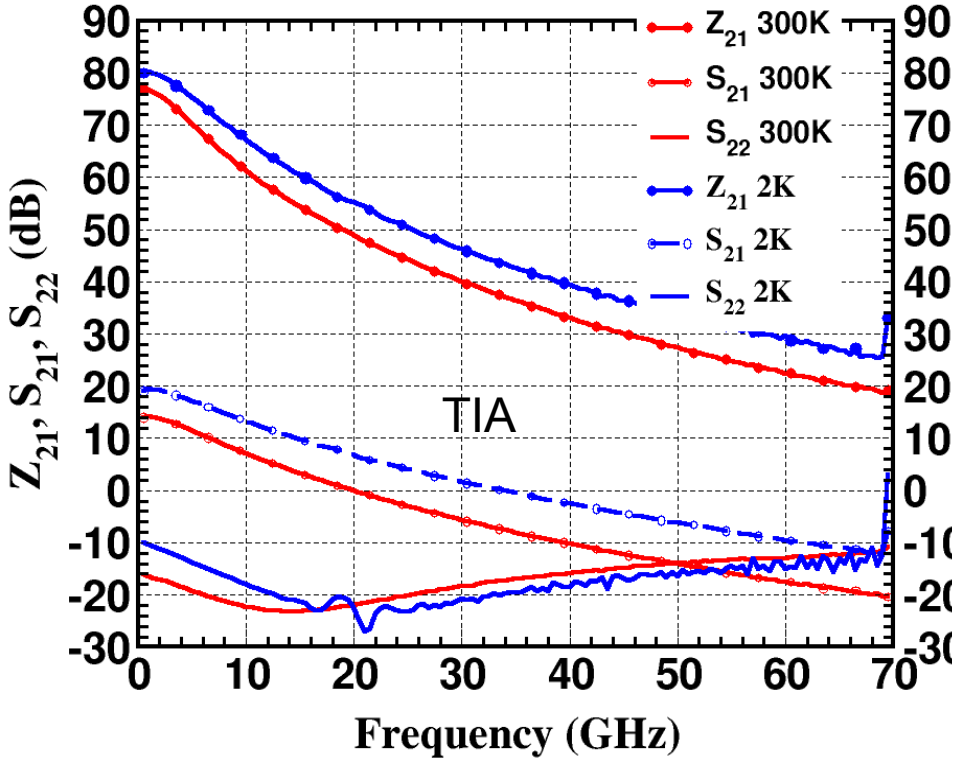
- Transistor and TIA performance improve at 2 to 3 K compared to 300 K
- V_t increases but is readjustable from back gate, channel undoped, => no kink
- Poly resistors and MOM caps vary by less than 5%
- T-line, inductor, transformer loss improve

[S. Bonen et al. EDL 2019]

HF Performance Improves at 2-3 K







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[S. Bonen et al. EDL 2019]

Conclusions

- Quantum processors are the most complex SoCs
  - Quantum dots
  - Analog-mixed signal circuits
  - Microwave/mm-wave circuits
  - Digital
- All 22nm FDSOI actives and passives work (better) at 2-70 K.
- Cryogenic testing slow and expensive
- Correlation between 4K and 300K testing must and can be established to reduce test time

Acknowledgments

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