Millimeter-Wave Integrated Silicon Devices: Active versus Passive –

The Eternal Struggle Between Good and Evil

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GOOD AND EVIL (1/2)

GOOD AND EVIL (2/2)

OUTLINE

- Silicon Technology Evolution
  - Active & Passive Devices
- Case Study: Low-Power Tuned mm-Wave LNA
  - Traditional Loss-Less Design Methodology
  - Advanced Loss-Aware Design Methodology
- Impact of Losses
  - Recalls on Noise Invariants
  - Results
- Conclusions

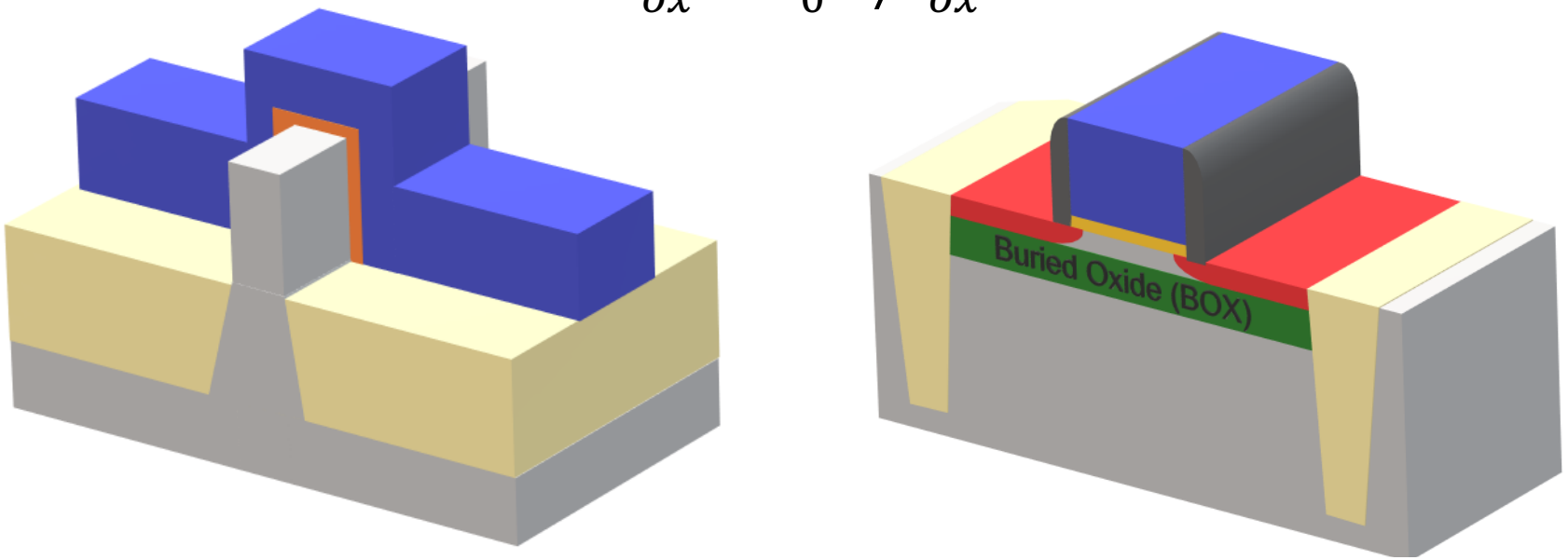
Si TECH EVO: CMOS TECHS

- Ultra-scaled device evolution driven by **charge control improvement** and **leakage current reduction**
- Two fully depleted (FD) techs emerged with **22/28nm** CMOS node (double patterned, high-k dielectrics, metal gate, strained silicon)

FinFET

$$C_{ox} = \varepsilon_0 \, k / t_{ox}$$

FD-SOI



[Cathelin, IEEE SSC Mag., 2017]

Si TECH EVO: FinFET

- **7nm FinFET** is the most advanced node in mass production
- Migration to **5nm** node already started:

Intel

— **10nm → 7nm**

Samsung

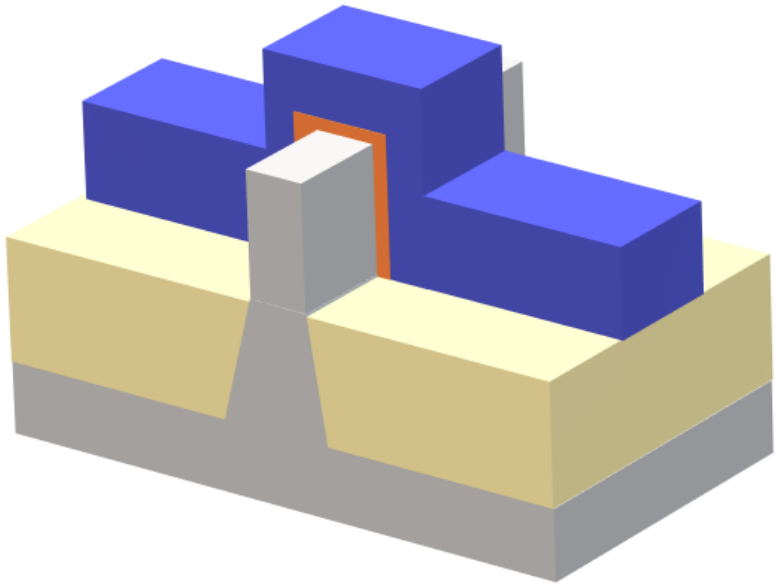
— **7LPP → 5LPE**

TSMC

— **N7P → N6 → N5 → N5P**

— **TeraPixel** taped out world's 1st TSMC 5nm chip

FinFET



Si TECH EVO: FD-SOI

- **CEA-Leti** & **STMicroelectronics (ST)** developed the 1st **FD-SOI** tech in mass production
- 3 foundries offer FD-SOI devices:

ST

— **28nm FD-SOI**

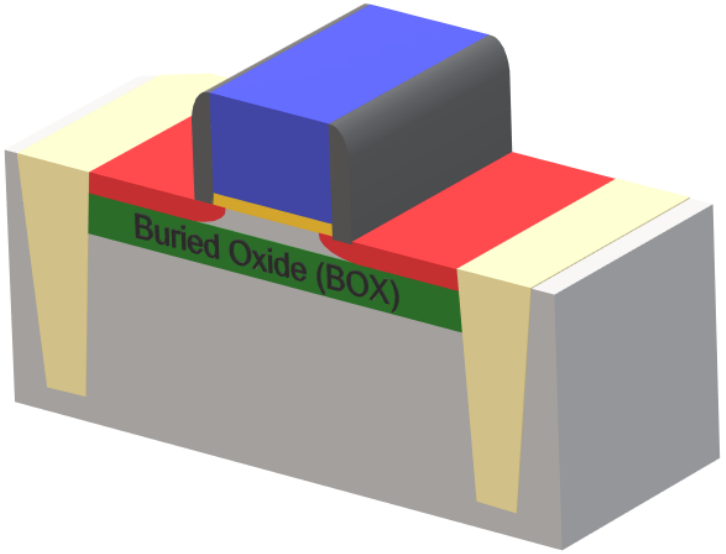
GlobalFoundries (GF)

— **22FDX® → 12FDX™**

Samsung

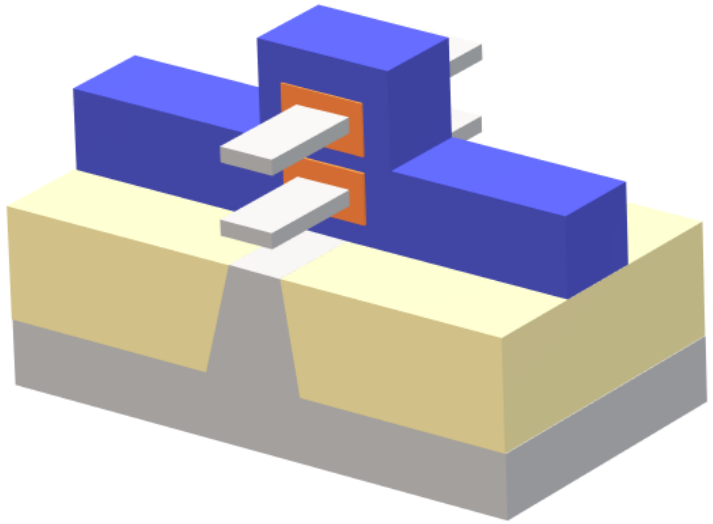
— **28FDS → 18FDS**

FD-SOI



Si TECH EVO: THE “LAST” TRANSISTORS

- **Samsung** will introduce a different transistor design starting from the **3nm** node
- The next transistor has already many names
  - **gate-all-around**
  - **multi-bridge channel**
  - **nano-beam**
  - **nano-sheet**



[Ye, Ernst, Khare, IEEE Spectrum, Jul. 2019]

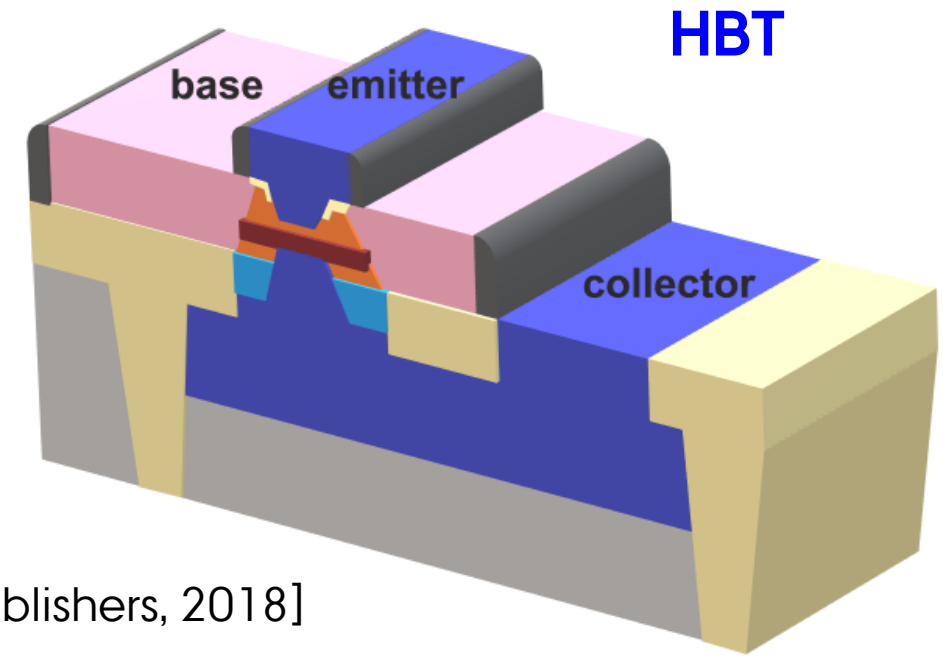
Si TECH EVO: SiGe BiCMOS TECHS

- Device evolution driven by **higher frequency operations** (f_T, f_{max}) and **integration with scaled CMOS devices**
- High-speed SiGe/SiGe:C Heterojunction Bipolar Transistors (HBTs) together with high-density CMOS

- $f_{max} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$

R_B: base resistance

C_{BC}: base-collector capacitance

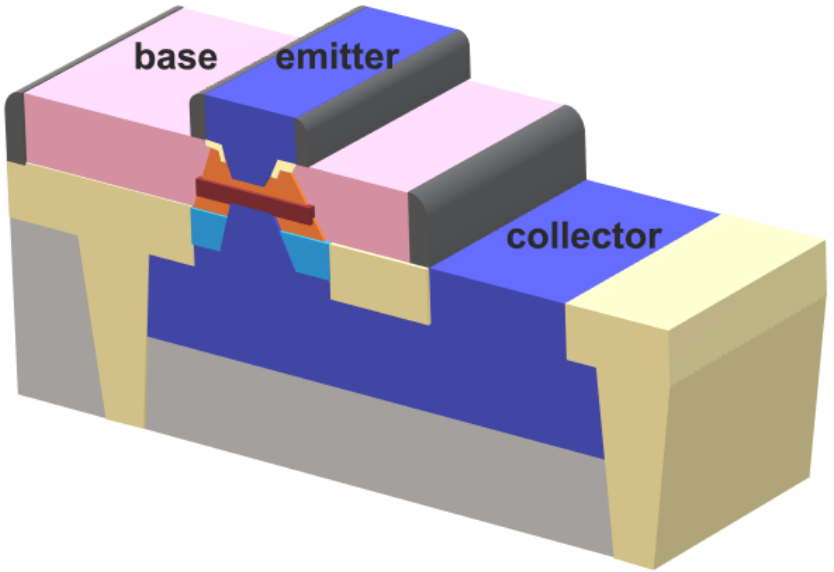


[Rücker, Heinemann, Ch. 1, River Publishers, 2018]

Si TECH EVO: SiGe BiCMOS TECHS (f_{max} ≥ 300 GHz)

- ST
  - BiCMOS055 (55nm)
- NXP
  - 90nm
- GF
  - 9HP (90nm)
- Infineon (IFX)
  - B11HFC (130nm)
- IHP
  - SG13 (130nm)
- TowerJazz
  - 130nm

HBT



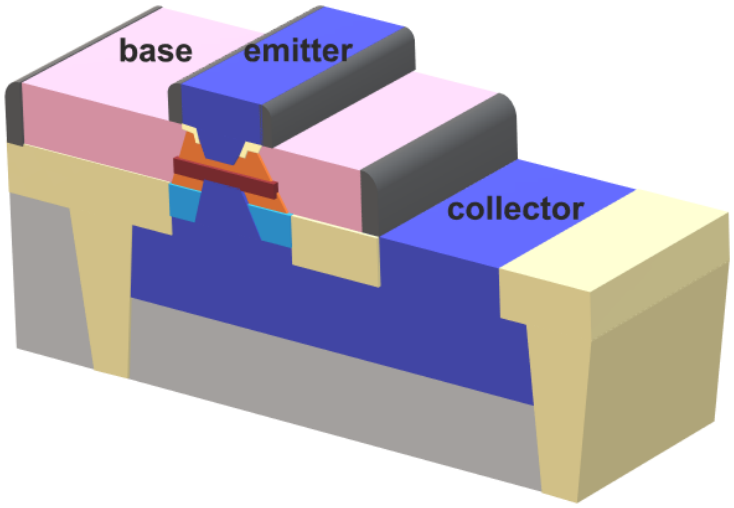
Si TECH EVO: SIGE BICMOS EU PROJECTS

- DOTSEVEN (IFX, IHP, et al.)
  - SiGe HBT with f_{max} of 700 GHz
- ECSEL TARANTO (ST, IFX, IHP, et al.)
  - HBT with f_{max} of 600 GHz integrated with high-density CMOS 130/90nm at IFX & 55/28nm at ST
  - f_{max} of 700 GHz compatibile with IFX & ST BiCMOS processes

Si TECH EVO: SiGe BiCMOS ADVANTAGES

- **HBT** f_T less sensitive to parasitic capacitance of metal layers
- More mature **back-end-of-line (BEOL)**, leading to better passives
- Lower **costs**

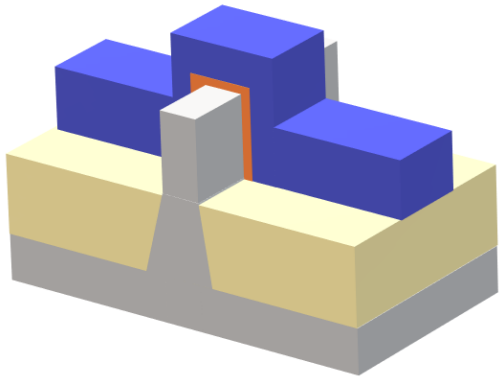
HBT

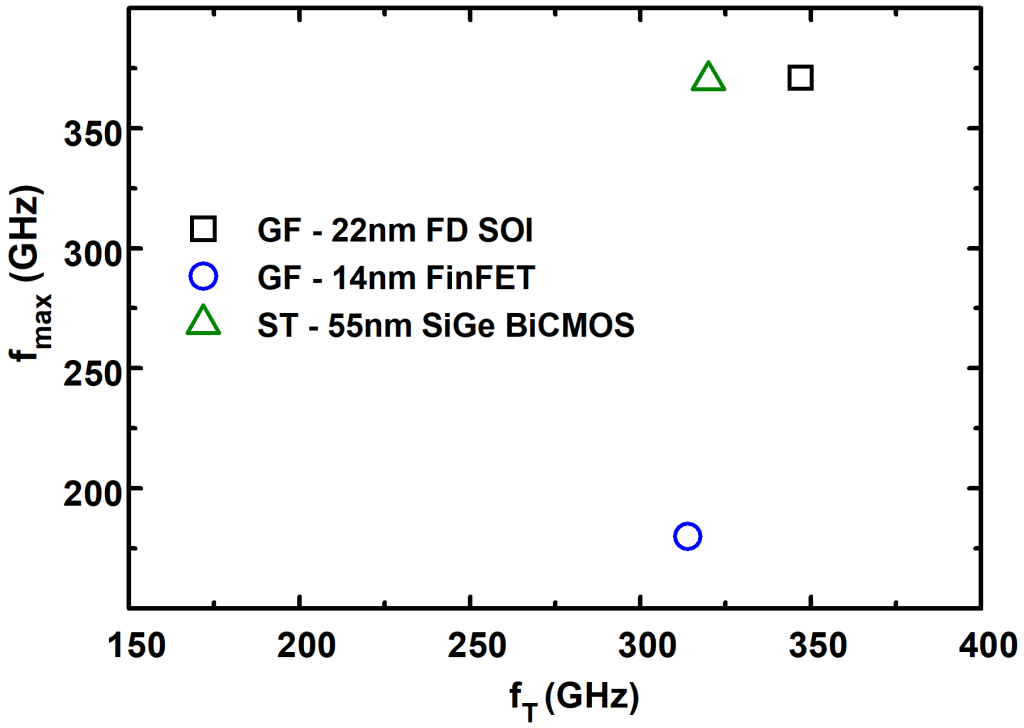


[Chevalier et al., IEEE BCICTS, 2018]

Si TECH EVO: FOMs

- **FinFET**, **FD-SOI** and **HBT** devices commercially available
  - f_T > 300 GHz
  - f_{max} > 150 GHz



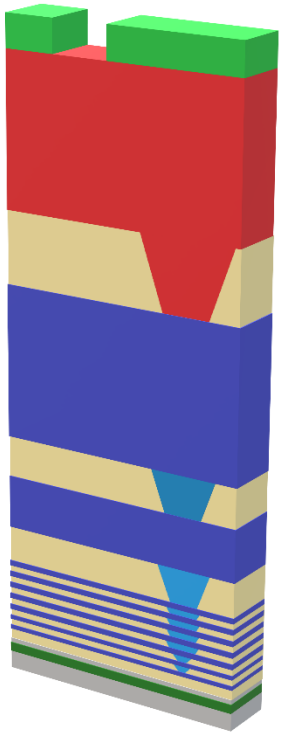


- **Active devices** have **outstanding performances** with **great potential for high-frequency applications**

[Ong et al., IEEE RFIC, 2018]
[Chevalier et al., IEEE IEDM, 2014]

Si TECH EVO: BEOL

FD-SOI

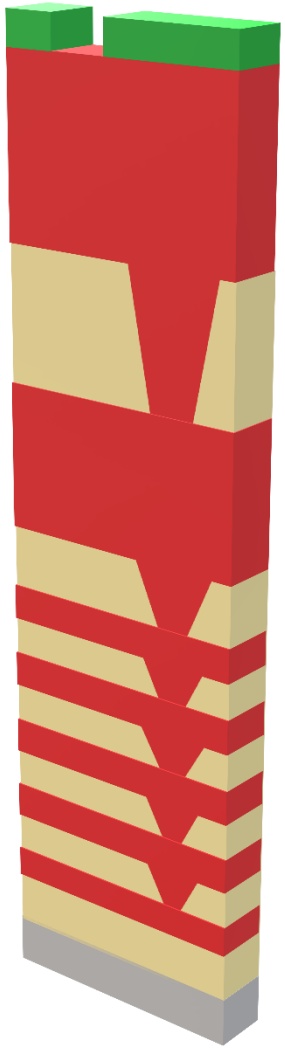


Passivation

Al

Cu

BiCMOS

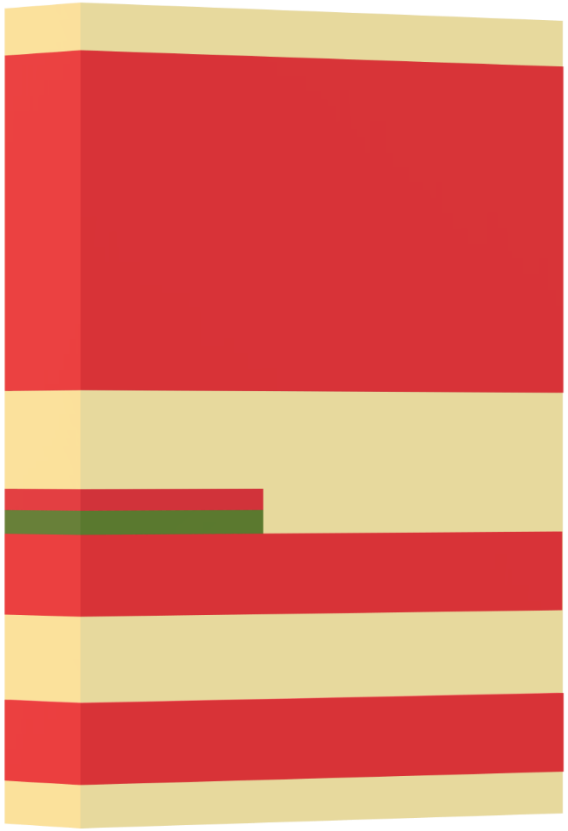


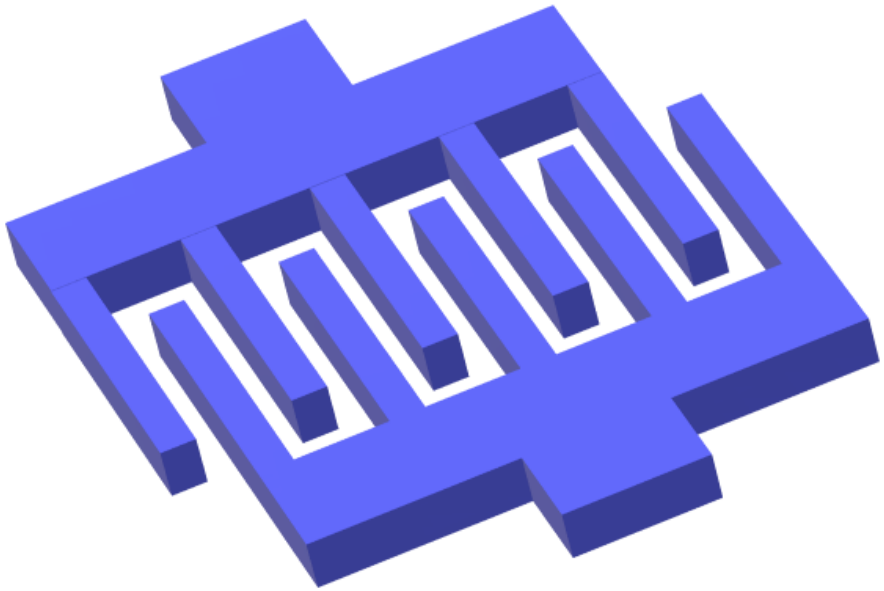
Si TECH EVO: CAPACITOR

MIM

MOM

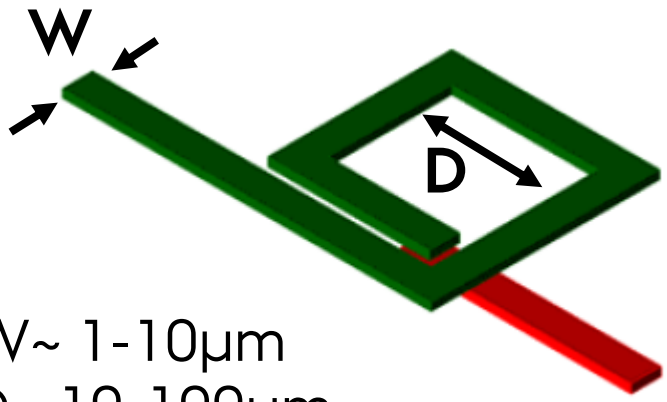
Metal
Insulator
Metal





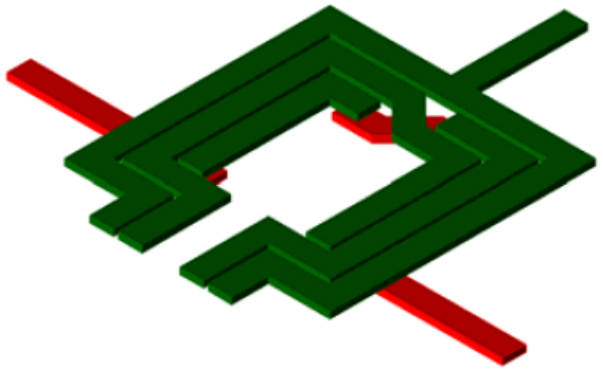
Si TECH EVO: INDUCTOR, TRANSFORMER, TX LINE

Inductor



W~ 1-10µm
D ~10-100µm
@60 GHz
L ~ 50-500pH
Q ~ 25-5

Transformer



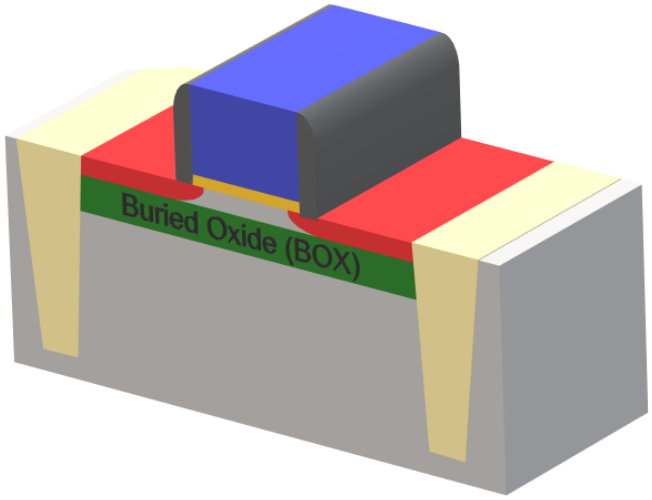
Co-planar waveguide

[Pepe, et al., "Design and test of W-band passive circuit components in 28nm bulk CMOS technology", 27th ISSC, 2016]

Si TECH EVO: mm-WAVE APPLICATIONS

- **These outstanding performances are enabling a plethora of applications**
  - high data-rate communications for next generation wireless networks (5G and beyond)
  - high-speed wireline communications
  - autonomous and near-autonomous vehicles
  - virtual reality
  - radio astronomy
  - Earth observations
  - satellite communications
  - **quantum computing**

FD-SOI



Si TECH EVO: LOSSES IN PASSIVES - THE REAL BOTTLENECK (1/2)

- Most of technology efforts are addressed to active devices
- **Losses in passive devices** are limiting the performances of **microwave and mm-wave ICs**
- To quantify the impact, we consider the case of **low noise amplifiers (LNAs),** among the most critical building blocks in high-frequency transceivers

Si TECH EVO: LOSSES IN PASSIVES - THE REAL BOTTLENECK (2/2)

- Most widespread theoretical approaches to LNA design are based on **lossless matching networks (MNs)**
- **Because of losses in MN**, the **theoretical bounds** to LNA performance **are far to be achieved**
- As a result, **the full potential of the active devices is not exploited**

CASE STUDY: LOW-POWER TUNED mm-WAVE LNA

- To study the impact of MN lossess on LNA performance, we compare **two LNA circuit topologies**, **each with its own design methodology**

- The LNAs are designed in a **0.13μm SiGe:C BiCMOS** technology commercially available

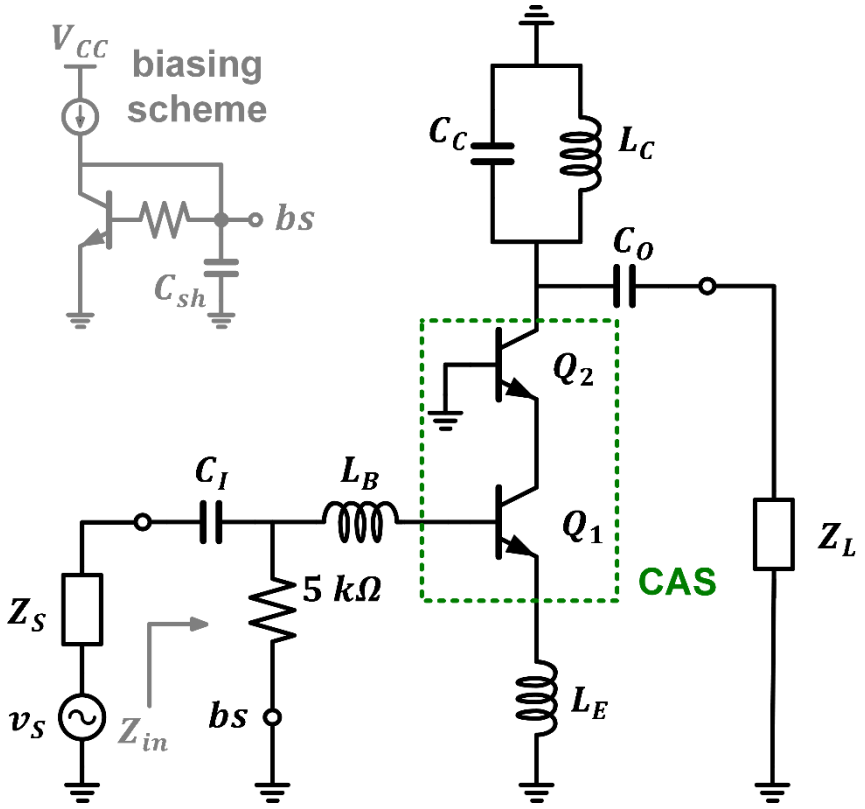
- We address the design of **high-frequency low power LNAs** at **60 GHz**

CASE STUDY: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (1/3)

- **Cascode with inductive degeneration**
  - most widespread topology for tuned LNAs
- **Lossless design methodology**
  - Area, L_E & L_B sized such that

$$Z_S = Z_{in}^* = Z_{ON}$$

Input Integrated Matching



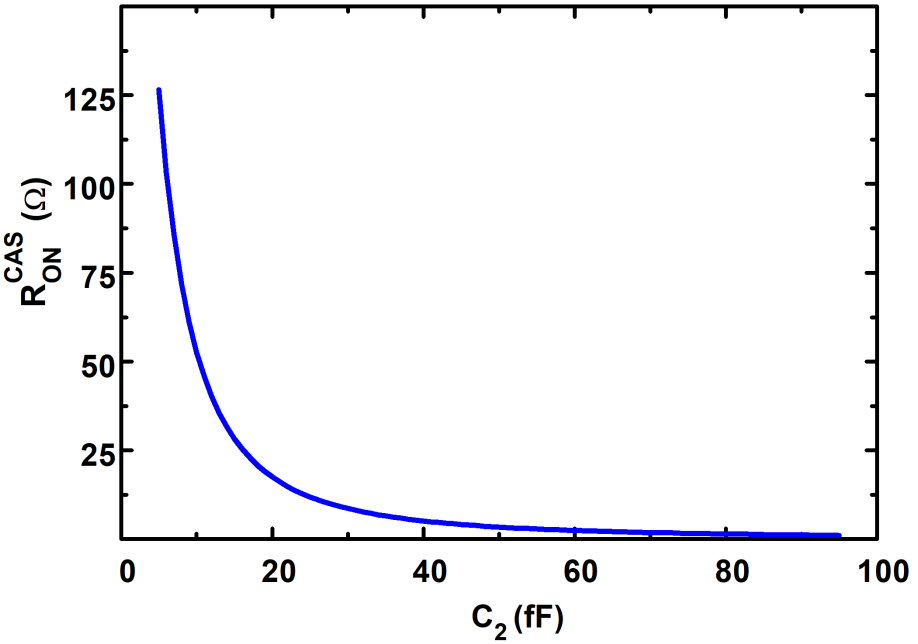
[Voinigescu et al., IEEE JSSC, 1997]

[Pepe et al., IEEE TCAS-I, 2018]

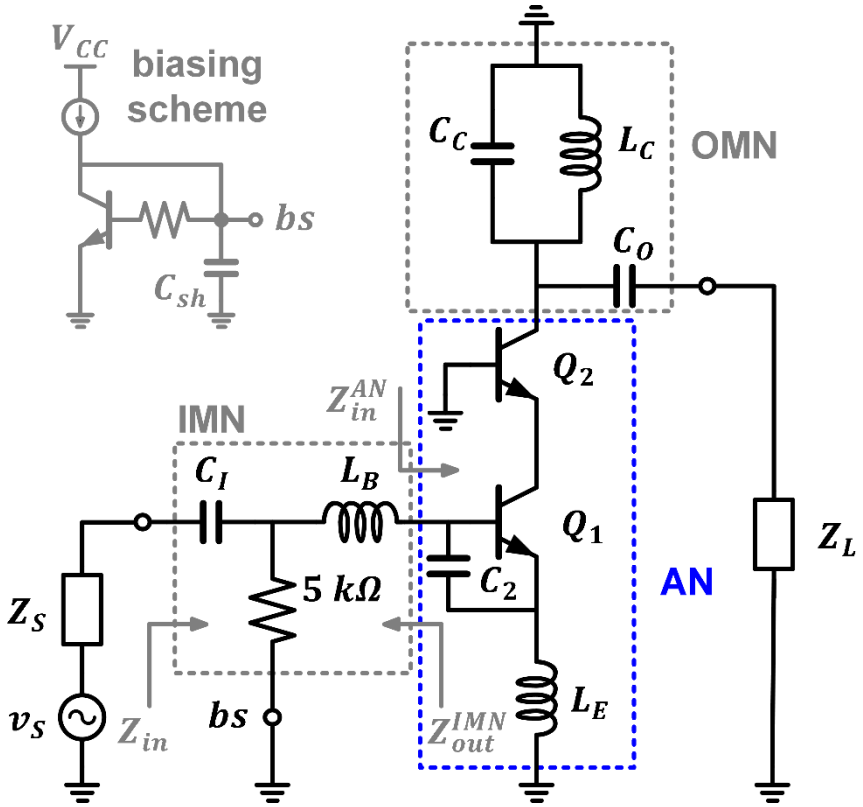
Z_{ON}: optimum-noise impedance
Z_S: source impedance
Z_{in}^*: conjugate of the input impedance

CASE STUDY: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (2/3)

- **Low-power design variation**
  - additional capacitor (C_2)
  - input integrated matching with smaller transistors



[Girlando, et al., IEEE TCAS-II, 1999]



AN: Active Network
IMN: Input MN
OMN: Output MN

CASE STUDY: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (3/3)

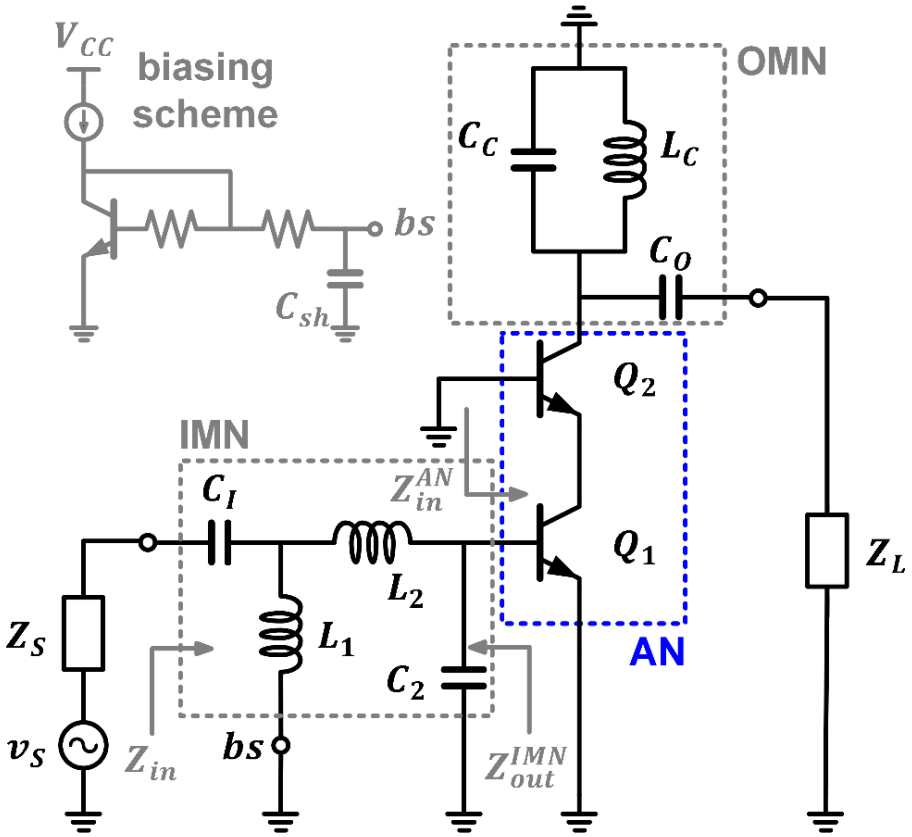
- **Input integrated matching** for maximum power transfer and minimum noise figure (IIM for MPmN)
  - $Z_{in} = Z_S^*$
  - $Z_{out}^{IMN} = Z_{ON}^{AN}$

- **MNs considered as lossless**

Z_{ON}^{AN}: AN optimum-noise impedance

CASE STUDY: ADVANCED LOSS-AWARE DESIGN METHODOLOGY (1/4)

- Recently, **we proposed an alternative circuit topology**
  - **IMN** with **2 capacitors & 2 inductors**
  - C_2-L_E feedback MN is removed
  - tailored to a **loss-aware design methodology**, also applicable to traditional LNA topology

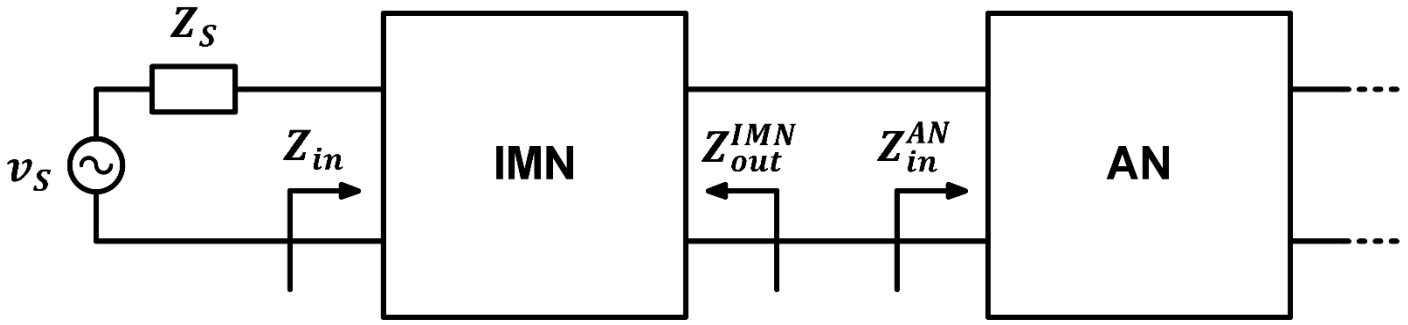


[Spasaro, et al., "The Theory of Special Noise Invariants", IEEE TCAS-I, 2019]
[Spasaro, et al., IEEE ICECS, 2018]

CASE STUDY: ADVANCED LOSS-AWARE DESIGN METHODOLOGY (2/4)

- **Because of the losses**, the reflection coefficients (Γ_{in}^{IMN}, Γ_{out}^{IMN}) at the two ports of IMN are unequal

$$\left|\Gamma_{in}^{IMN}\right| \neq \left|\Gamma_{out}^{IMN}\right| \Rightarrow \text{If } Z_{in} = Z_S^*, \text{ then } Z_{out}^{IMN} \neq \left(Z_{in}^{AN}\right)^*$$



⇒ **IMN losses** can be **exploited to change** Z_{out}^{IMN}

CASE STUDY: ADVANCED LOSS-AWARE DESIGN METHODOLOGY (3/4)

- LNA equivalent noise temperature T_N, neglecting OMN noise

$$T_N \approx T_0 \left(\frac{1}{\boldsymbol{G_A^{IMN}}} - 1 \right) + \frac{T_{Nmin}^{AN}}{\boldsymbol{G_A^{IMN}}} \left(1 + \Delta\theta_R^{AN} \frac{\left| Z_{ON}^{AN} - \boldsymbol{Z_{out}^{IMN}} \right|^2}{4 R_{ON}^{AN} \boldsymbol{R_{out}^{IMN}}} \right)$$

- IMN design goals
  - If $Z_{out}^{IMN} = Z_{ON}^{AN}$, AN noise contribution is minimized
  - To minimize IMN noise contribution, IMN available gain (G_A^{IMN}) must be maximized

G_A^{IMN} and Z_{out}^{IMN} are not independent ⇒ trade off is needed

$T_{Nmin}^{AN}, \Delta\theta_R^{AN}, Z_{ON}^{AN}$: AN noise parameters

CASE STUDY: ADVANCED LOSS-AWARE DESIGN METHODOLOGY (4/4)

- **Input integrated matching for maximum power transfer and minimum cascade noise (IIM for MPmCN)**
  - $Z_{in} = Z_S^*$
  - the equivalent noise temperature of the cascade of IMN and AN is minimized

- **General guideline: IMN must comprise at least 3 components**
  - C_2, L_1, L_2 and C_l

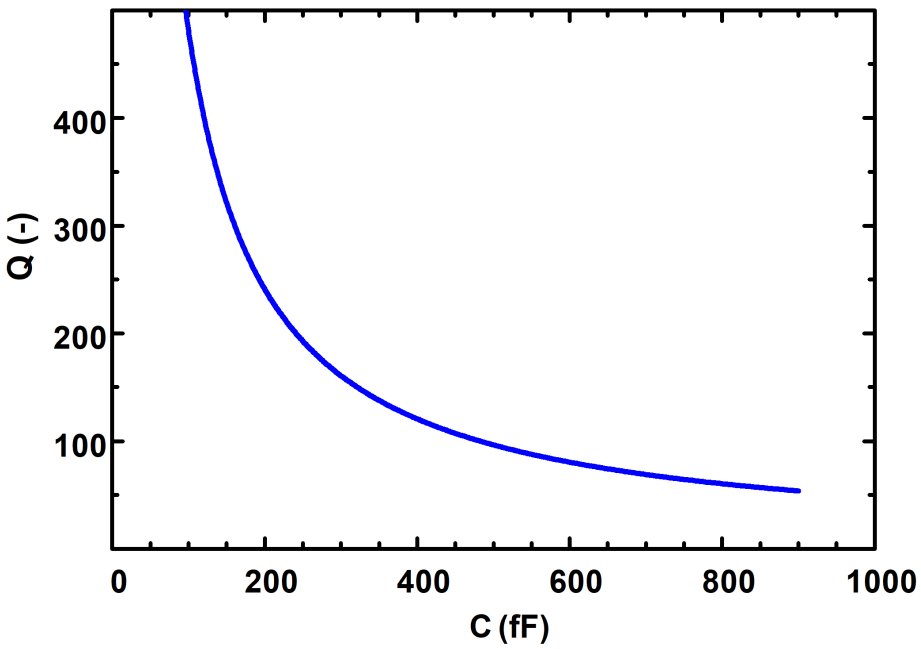
[Spasaro, et al., IEEE TCAS-I, 2019]

CASE STUDY: ASSUMPTIONS (1/2)

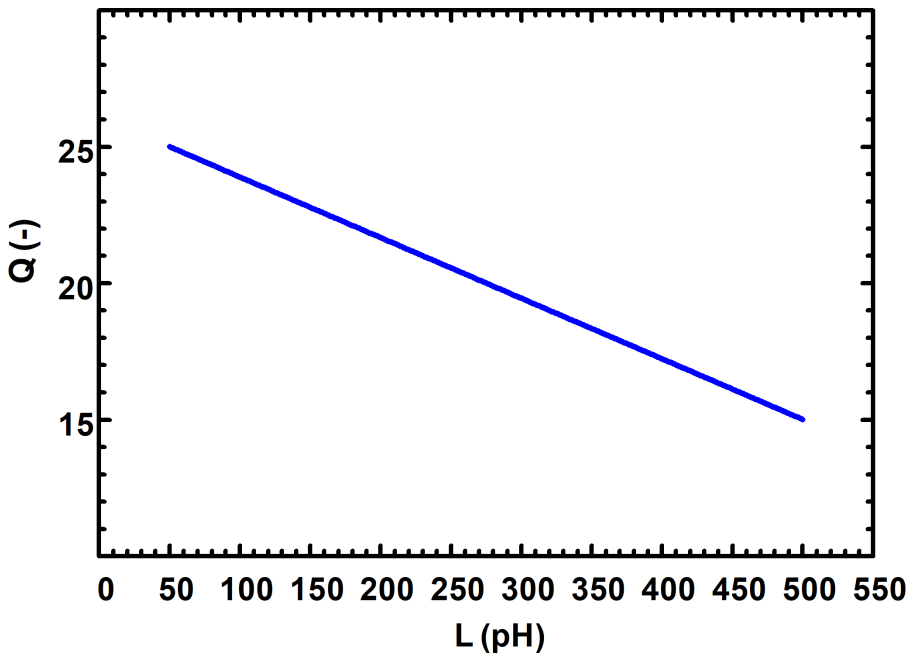
- The two LNAs have:
  - same transistor biasing: current density minimizing cascode F_{min}
  - minimum size transistors, to minimize power consumption (760μW from 2V supply)
  - equal values of C_O, C_C, and L_C (OMN designed for maximum power transfer)

CASE STUDY: ASSUMPTIONS (2/2)

Capacitors



Inductors



- Passive components
  - **MIM capacitors**, available within the design kit
  - linear regression of the **Q** of **inductors** between **25 for 50 pH** and **15 for 500 pH** (@ 60 GHz)

IMPACT OF LOSSES: BRIEF RECALLS ON NOISE INVARIANTS (1/2)

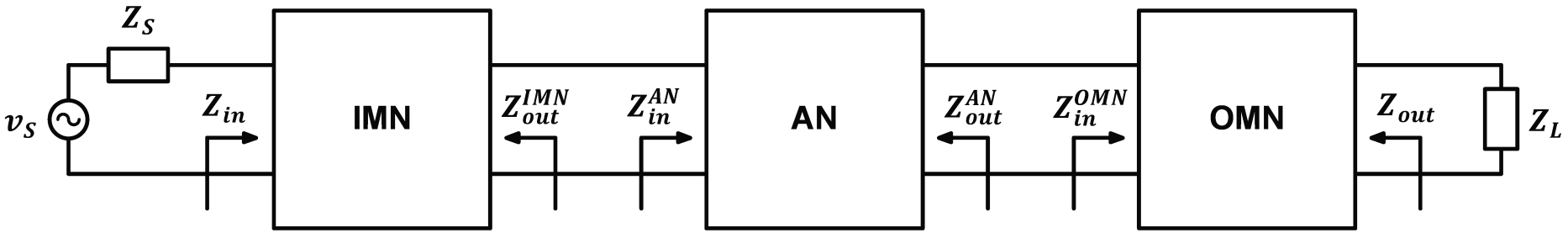
- **How can we assess the impact of MN losses?**

- By focusing on quantities that lossless MNs keep unchanged: **invariants**

- An invariant which measures the noise performance of an LNA is a **noise invariant**

IMPACT OF LOSSES: BRIEF RECALLS ON NOISE INVARIANTS (2/2)

LNA with lossless reciprocal feedforward MNs

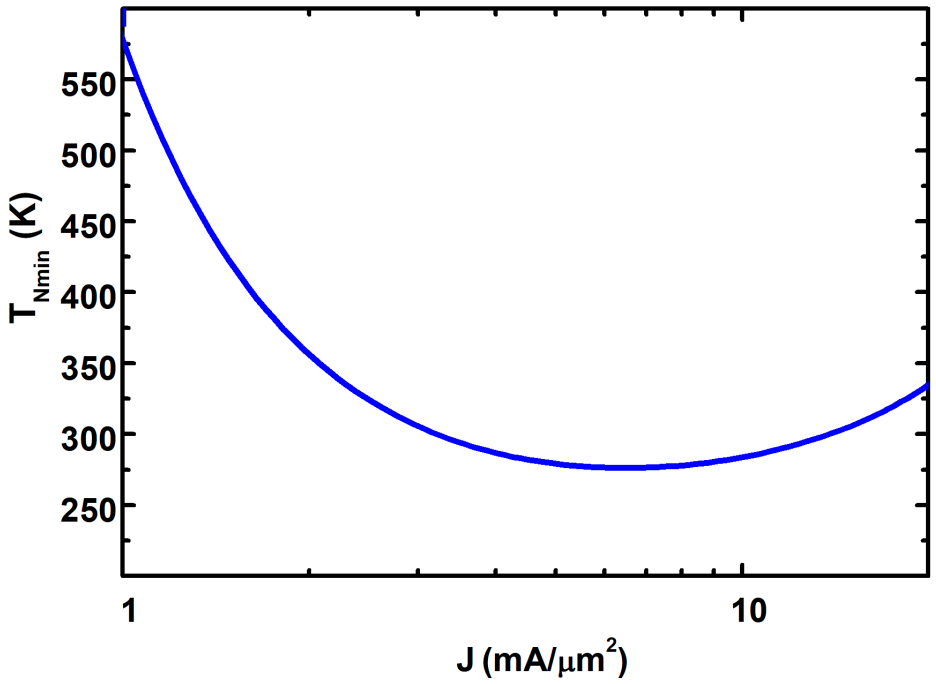


- The minimum equivalent noise temperatures of the LNA (T_{Nmin}) and AN (T_{Nmin}^{AN}) are equal

$$T_{Nmin} = T_{Nmin}^{AN}$$

$\Rightarrow T_{Nmin}^{AN}$ is a noise invariant

IMPACT OF LOSSES: CASCODE AMPLIFIER



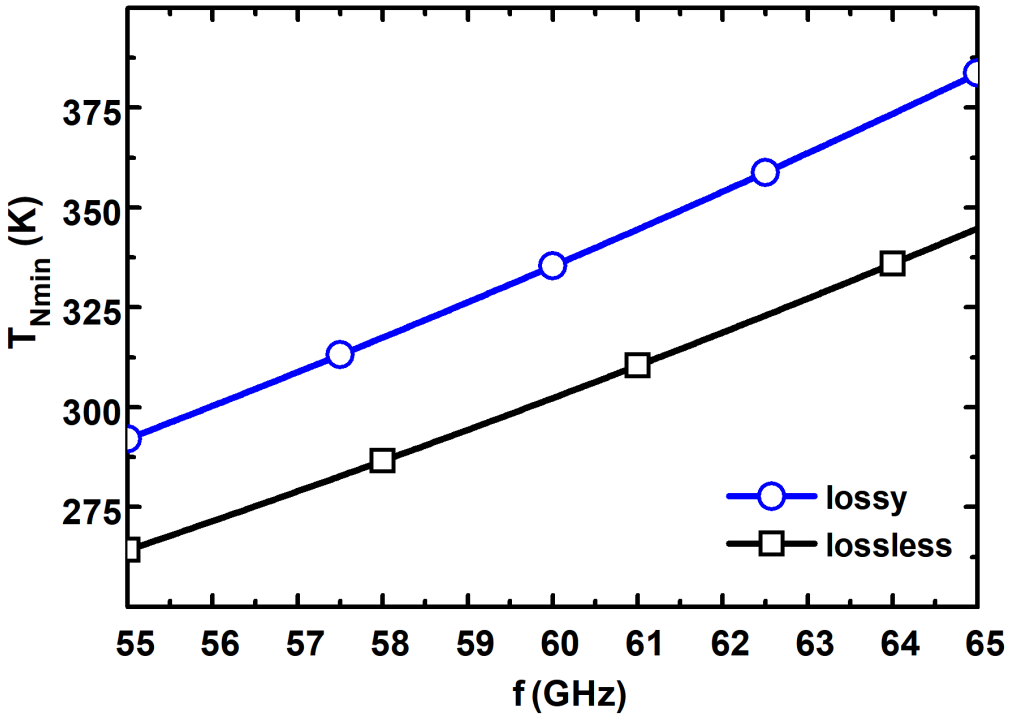
- The minimum equivalent noise temperature T_{Nmin}^{CAS} of the **cascode** amounts to **276 K**
- The corresponding current density is equal to **6.6 mA/μm²**

IMPACT OF LOSSES: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (1/3)

- The design of C_2-L_E **feedback** leads to an increase in T_{Nmin}^{AN} with respect to T_{Nm}^{CAS}.

- With lossless feedback MN, $T_{Nmin}^{AN} = 303K$

- With lossy feedback MN, $T_{Nmin}^{AN} = \mathbf{336K}$



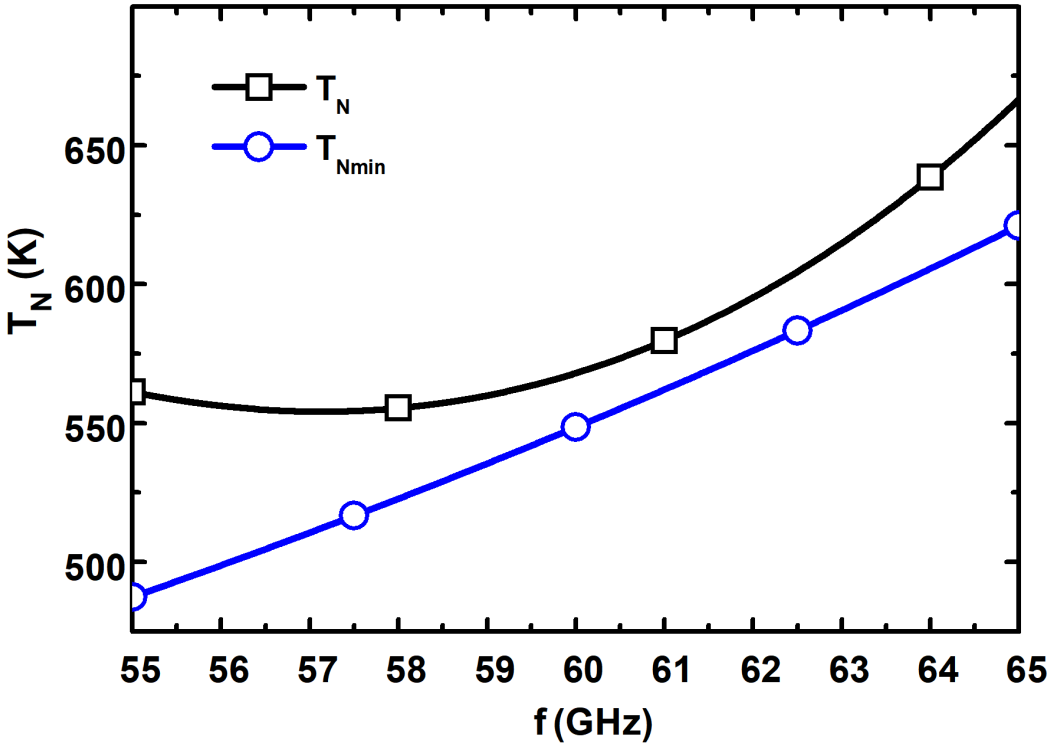
⇒ 11% increase of T_{Nmin}^{AN} due to feedback losses

IMPACT OF LOSSES: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (2/3)

- The LNA design is completed by sizing IMN and OMN

- With lossless feedback MNs, T_{Nmin} would be equal to T_{Nmin}^{AN}

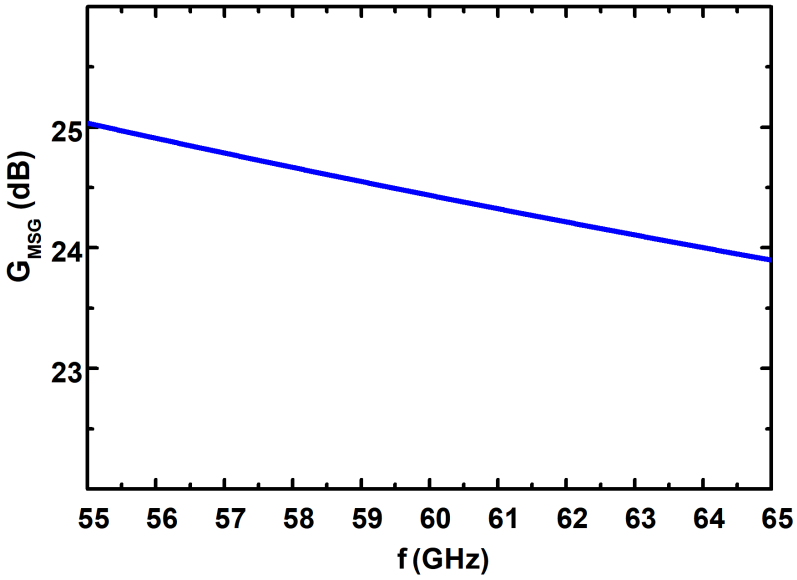
- Losses in IMN and OMN raise T_{Nmin} to **548K**



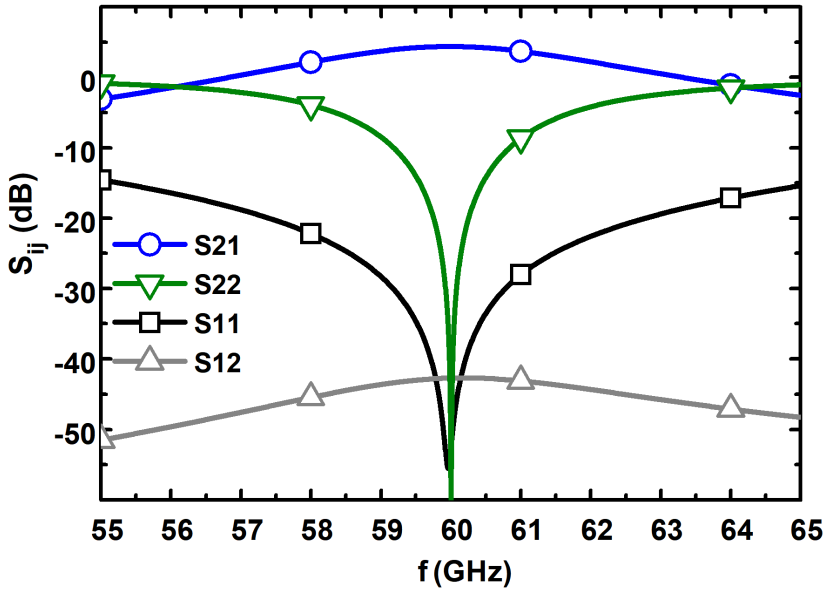
⇒ 98.5% increase of T_{Nmin} with respect to T_{Nmin}^{CAS}

IMPACT OF LOSSES: TRADITIONAL LOSS-LESS DESIGN METHODOLOGY (3/3)

AN maximum stable gain



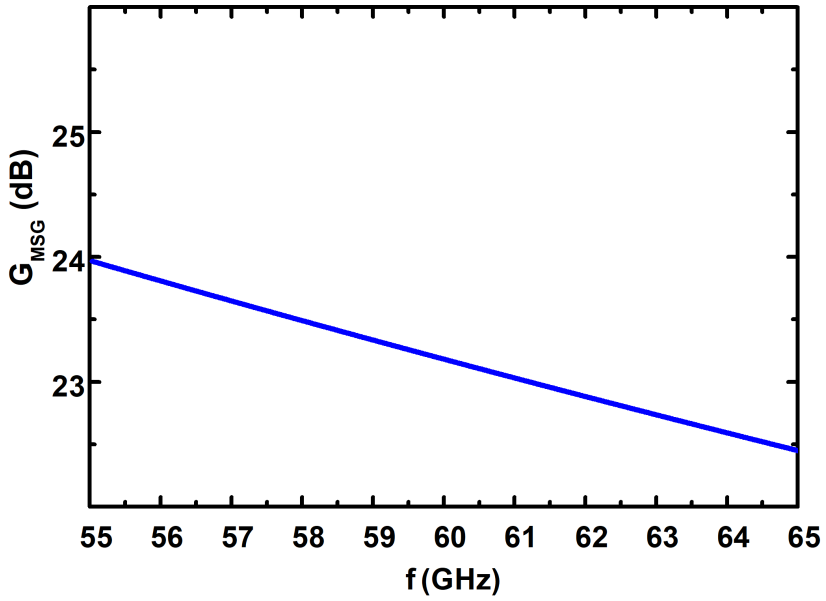
LNA S-parameters



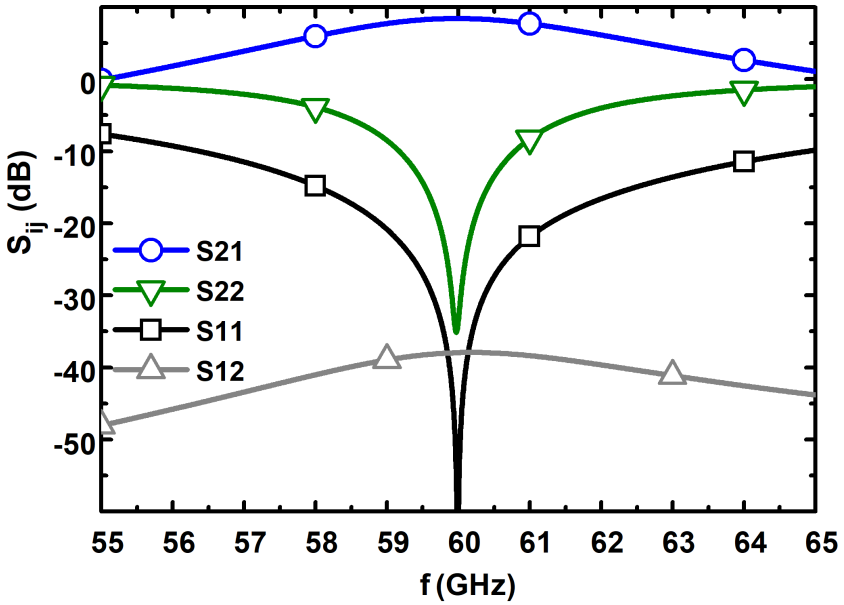
- Despite AN maximum stable gain $\left(G_{MSG}^{AN}\right)$ of **24.4 dB**, MN losses reduce **S_{21}** to **4.4 dB !**
- **IMN and OMN losses spoil transistor gain potential**

IMPACT OF LOSSES: ADVANCED LOSS-AWARE DESIGN METHODOLOGY

AN maximum stable gain

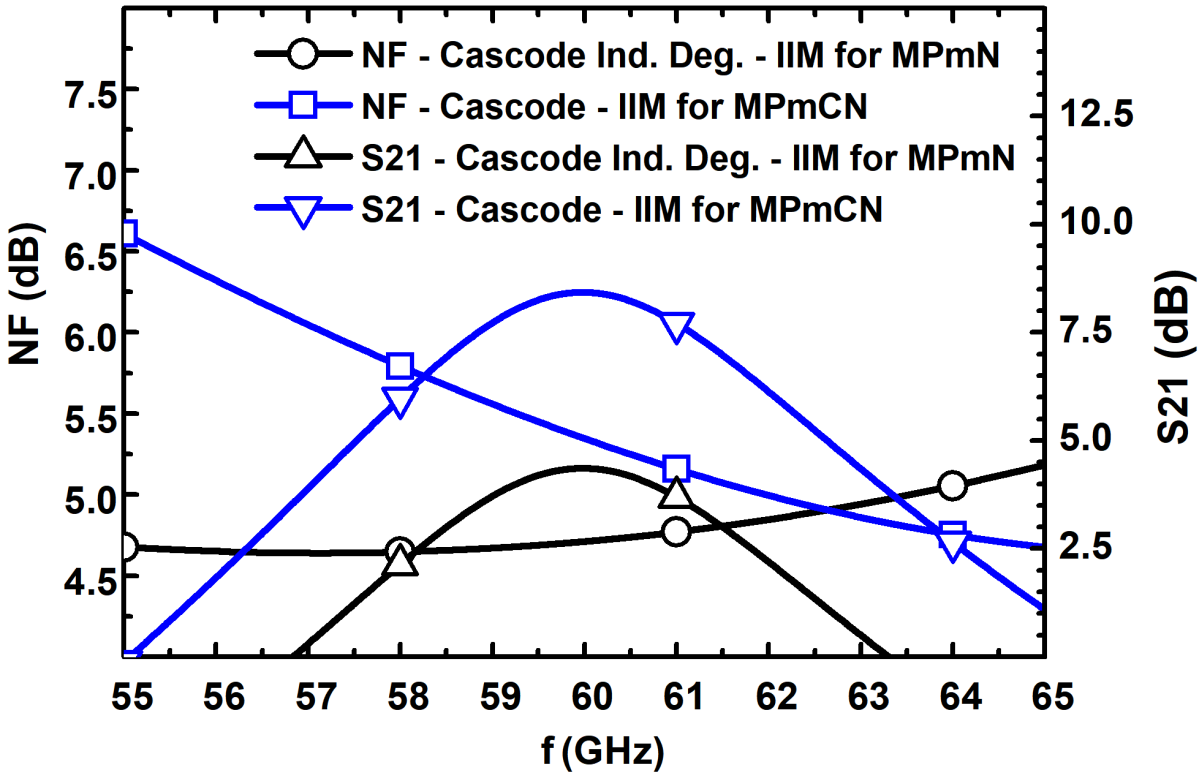


LNA S-parameters



- Despite AN maximum stable gain $\left(G_{MSG}^{AN}\right)$ of **23.2 dB**, MN losses reduce S_{21} to **8.4 dB**
- **The loss-aware methodology reduces the impact of losses**

IMPACT OF LOSSES: COMPARISON



- **IIM for MPmCN** achieves a superior gain **$S_{21}$of 8.4 dB** with a slightly degraded NF

IMPACT OF LOSSES: RESULTS

- As **IIM for MPmCN** improves **power-added noise temperature** (MT_0) and **gain-noise excess** (ϵ_{GN}), the worse NF is well compensated by the higher gain

Topology	S_{21}	NF	T_N	MT_0	iP_{1dB}	ϵ_{GN}
Cascode Ind. Deg.	4.4 dB	4.7 dB	568 K	897 K	-9 dBm	-0.3 dB
Cascode	8.4 dB	5.3 dB	703 K	**821 K**	-13 dBm	**3.1 dB**

$$MT_0 = T_N/(1 - 1/G_A) \qquad \epsilon_{GN} = S_{21}[dB] - NF\ [dB]$$

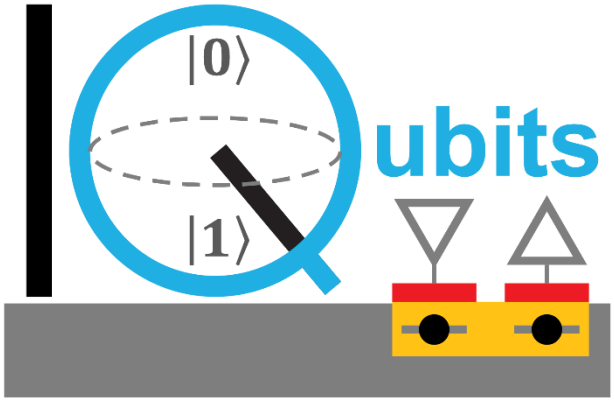
CONCLUSIONS (1/2)

- The evolution of silicon technologies has led to transistors with excellent performance for operation at mm-waves
- However, losses in passive devices impede full exploitation of transistors potential in mm-wave IC design
- We focused on mm-wave LNA design, unveiling (quantitatively) the dramatic performance degradation due to MN losses and the benefits of loss-aware design strategies

CONCLUSIONS (2/2)

- The results indicate the strong **need of further technology advances towards better passives**
  - new materials
  - new technology processes
- Also, **loss-aware design methodologies are a must** and key to design ICs and systems **in the mm-wave frequency range and beyond**

ACKNOWLEDGMENTS

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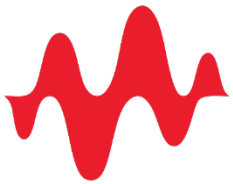
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