# Engineering Solid-State Qubits Structures for High-Temperature Silicon Quantum Computing Through Multi-Scale Simulations

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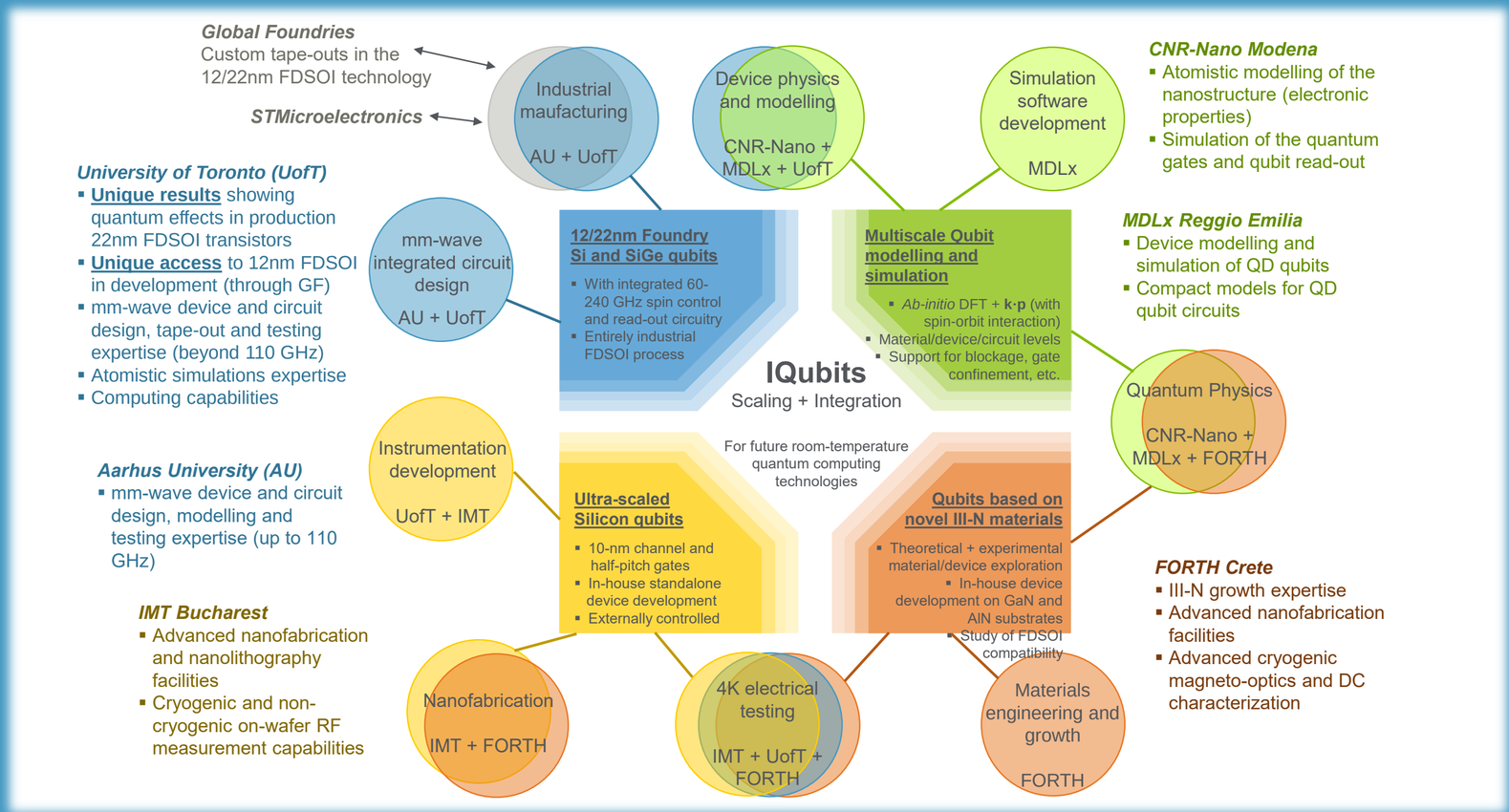
## Abstract

Quantum computing is today considered one of the key future technologies that will lead the next revolution of electronics. Among the different possible physical platforms, semiconductor-based qubits provide several advantages, not least their integration with electron/hole spin control/readout circuitry on the same die, though nowadays they require extremely low temperatures (e.g. 100 mK) to be reliably operated. Nevertheless, the scaling of CMOS technology is expected to reach 5 nm gate length and less than 2 nm channel cross-section by the year 2030. This will enable tunneling-based coupled quantum-dot (QD) devices to be operated at much higher temperatures, expecting to reach coupling energies on the order of 0.25-1 meV corresponding to control frequencies in the 60-240 GHz range, suitable for operation at 3–12 K. Since huge efforts are required to identify and engineer optimal structures, such as device geometry and employed materials, physics-based simulations are critical to this purpose.

We use Ginestra™ – a commercial multi-scale device simulation software developed by Applied Materials – as a test-bed for material characterization, simulation of electrical properties and device optimization, which makes it a unique simulating tool. As an industrial partner of the European FET Open Project IQubits, we will support the development of future silicon-based technology for the realization of Si, SiGe and III-Nitride QDs, their scalability to nanometric scale and the projection towards room-temperature quantum computing.

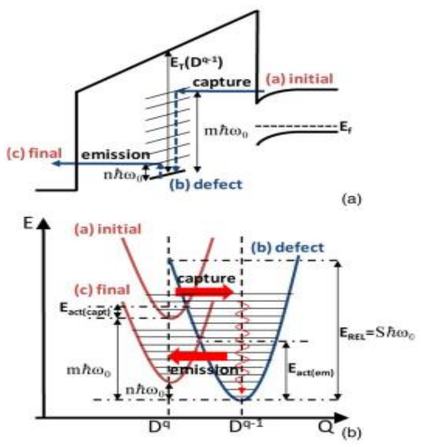




## Key innovations

- **integration of qubits and electronics on the same die**: based on commercial 22nm FDSOI CMOS foundry technology
- **demonstration of qubit and qubit ICs with operation above 3 K**: scalability of the qubits to 10nm dimensions. Prove the suitability 300K operation through atomistic simulations that at 2nm
- **Silicon-based qubits**: realization of series-stacked n- and p-MOSFET with multiple gates, where QDs form in the thin undoped semiconductor film below each top gate
- **III-N electron and hole spin qubits**: better prospect than Si and SiGe qubits with larger coupling energy and mode energy splitting
- **60-240GHz spin control and readout circuits**: short, 10-20ps spin control pulses, resulting in large ratios between the gating and the decoherence times
- **thermal noise filtering**: connecting many identical qubits in parallel to minimize readout errors

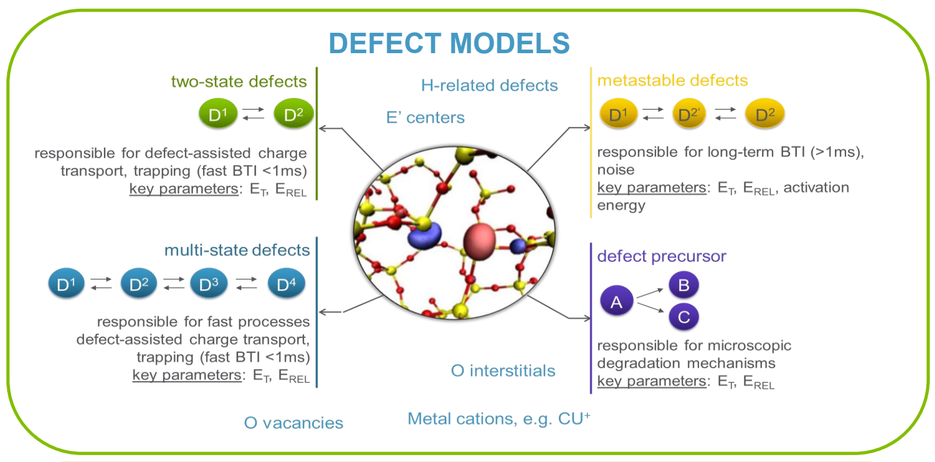
## INSIDE GINESTRA™

### CHARGE TRANSPORT

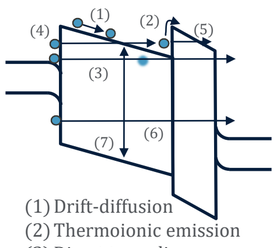



- Standard **semiconductor transport equations** for band carriers
- **Trap-Assisted Tunneling** (TAT) transport
- **Multiphonon theory**
- Variety of **defects** (e.g., vacancies, ions, …)

### DEFECT MODELS




### TUNNELING AND OTHERS



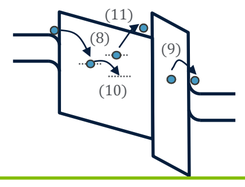
(1) Drift-diffusion
(2) Thermoionic emission
(3) Direct tunneling
(4) Electrode-band tunneling

### CARRIERS TRANSPORT

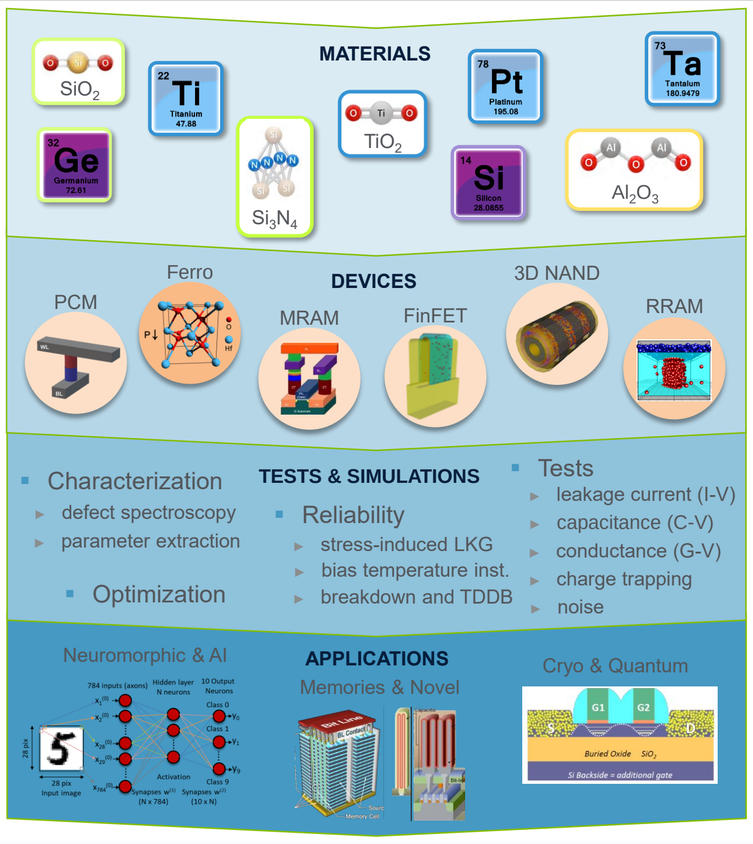
(5) Intra-band tunneling
(6) Band-to-band tunneling
(7) Local generation-recombination

### TRAP-ASSISTED

(8) Electrode-to-trap capture
(9) Trap-to-electrode emission
(10) Trap-to-trap transition
(11) Trap-to-band transition

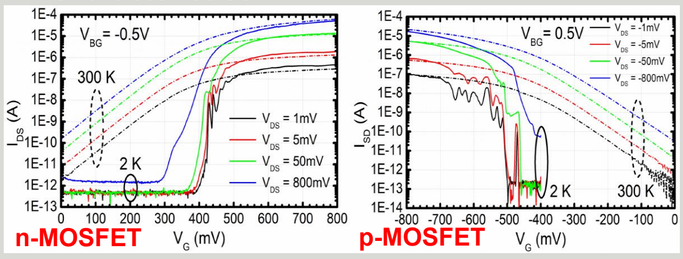


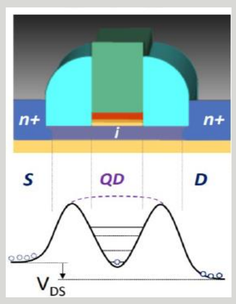
## GINESTRA™ CAPABILITIES

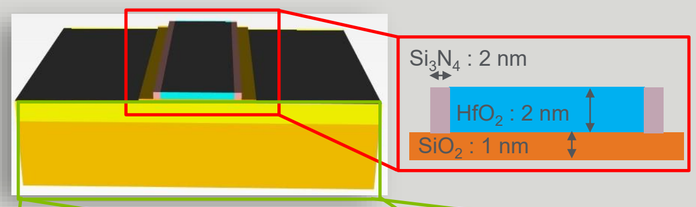


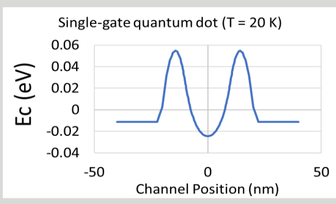

## Single Gate n- and p-MOSFET FDSOI

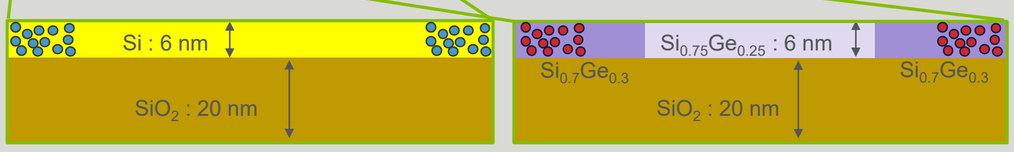
### I-V characteristics



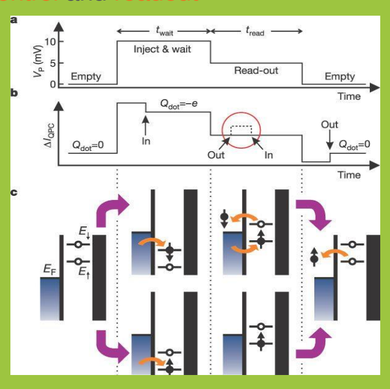

Electron-spin qubit

Hole-spin qubit

## GINESTRA™ FOR IQubits

- Quantization of energy levels
- Resonant tunneling for carriers transport
- Optimization of structures' geometry
- Optimization of voltages and materials
- Spin-orbit mechanism for hole-spin qubits
- Compact model for qubit operations and circuit simulations

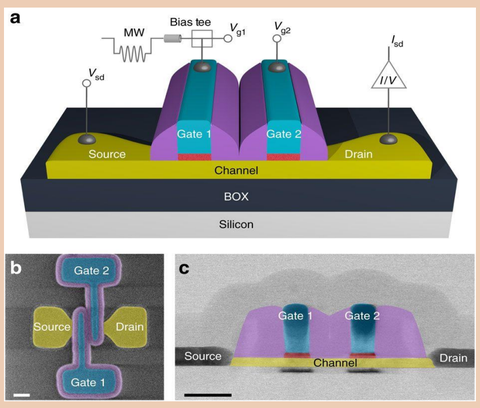
Manipulation of the qubits: initialization, control and readout



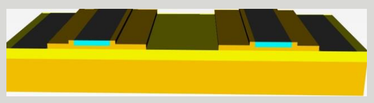
*Single-shot read-out of an individual electron spin in a quantum dot*, J. M. Elzerman *et al.*, *Nature*. **430**, 431 (2004)

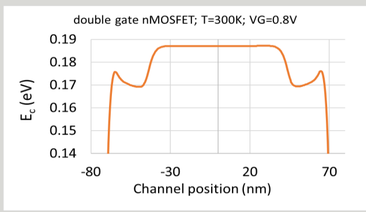
## Double Gate MOSFET FDSOI

Design and fabrication of a double gate structure for DQDs




*A CMOS Silicon Spin Qubit*, R. Maurand *et al.*, *Nat. Comm.* **7**, 13575 (2016)



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APPLIED MATERIALS
make possible