RMo2C-4

# Design Considerations for Spin Readout Amplifiers in Monolithically Integrated Semiconductor Quantum Processors

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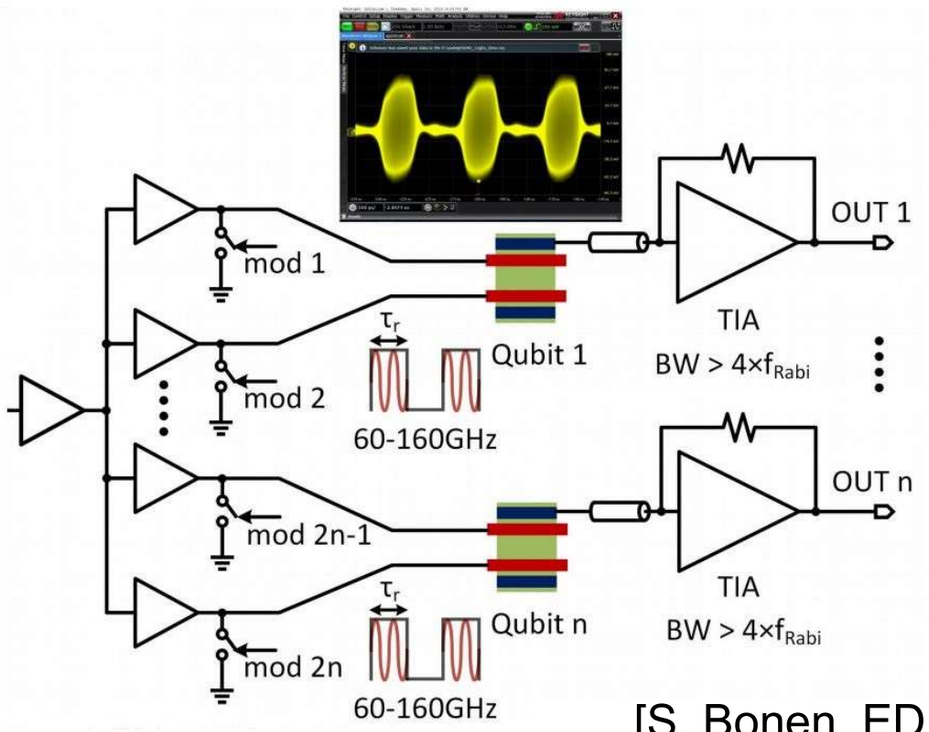
# Outline

- Introduction
- Technology Characterization
- Readout Amplifier Design
- Measurements
- Conclusion

# Key Novel Ideas

- Monolithic Quantum Processors in production CMOS
  - Qubits + control and readout electronics **on the same die!**

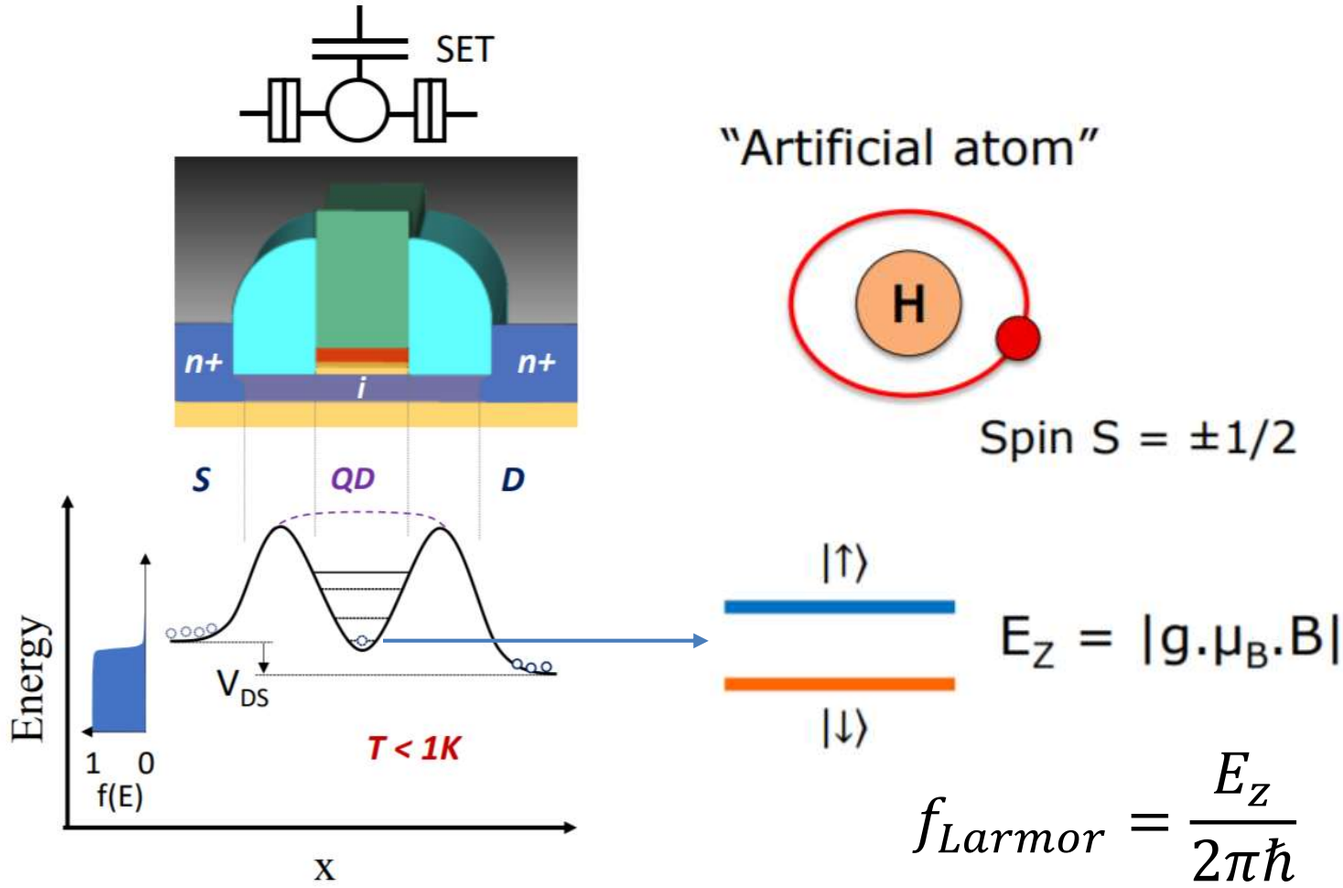
- The Qubit = minimum-sized transistor in sub-threshold
- Readout electronics → transistors in saturation
- All operating at 2 - 4 K




[S. Bonen, EDL 2019]

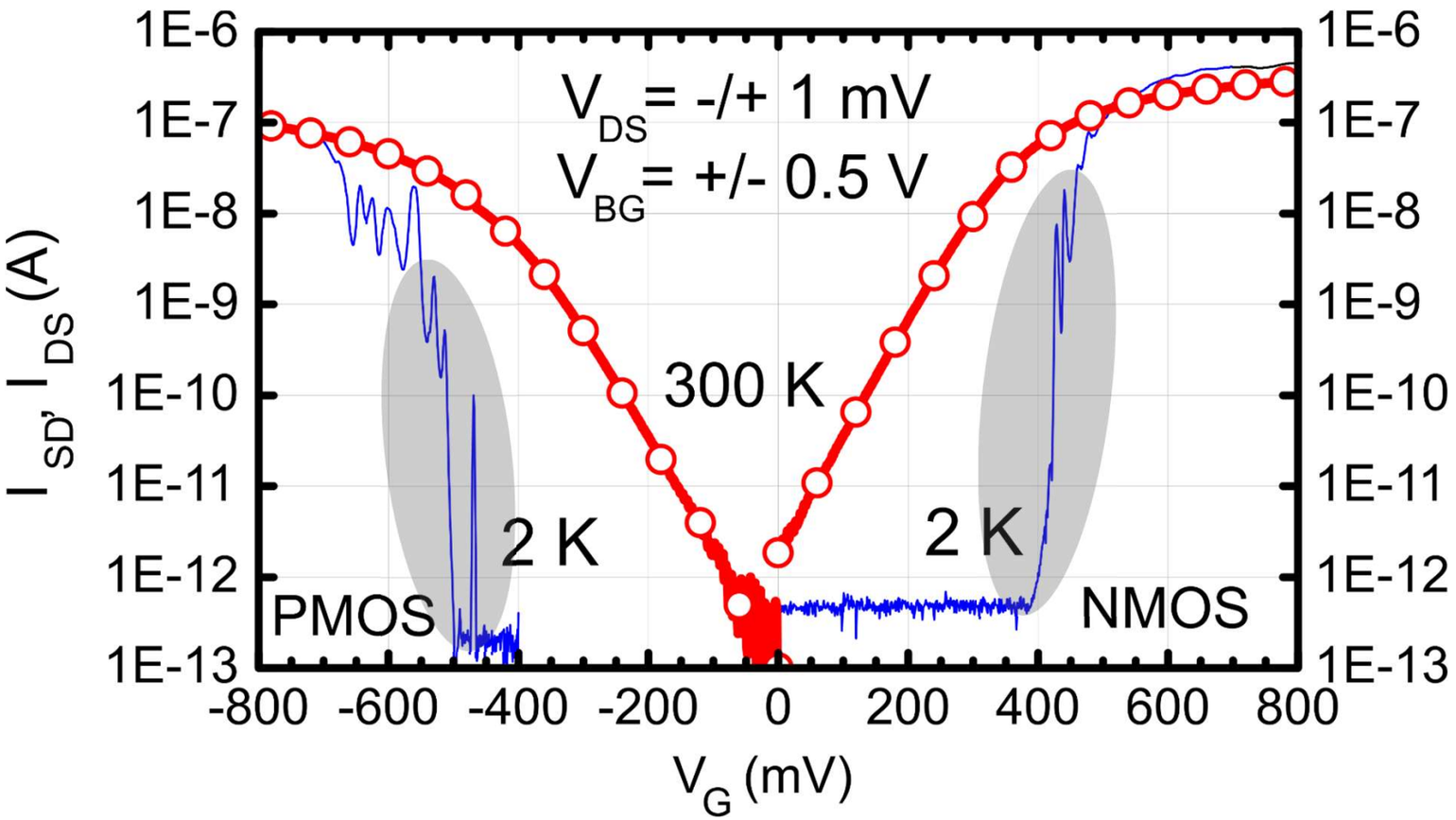
# From FDSOI MOSFET to Quantum Dot to Qubit

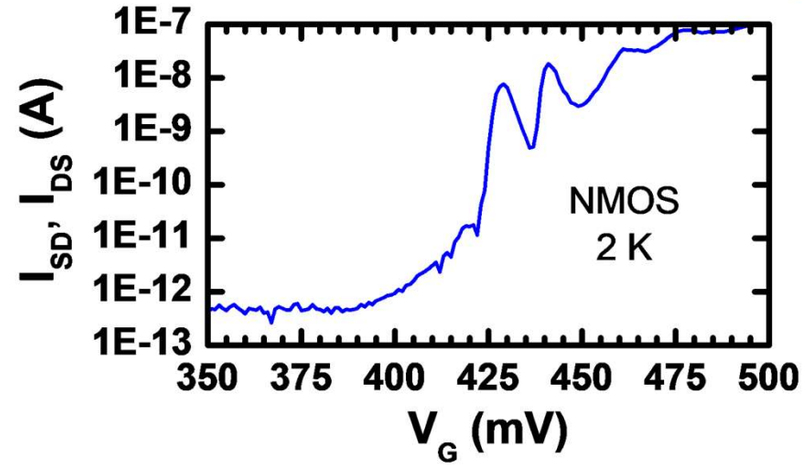
- $E_2 - E_1 >>$ kT
- $B$ splits $E_1$ into distinct spin up and spin down energy levels
- Qubit encoded in spin state

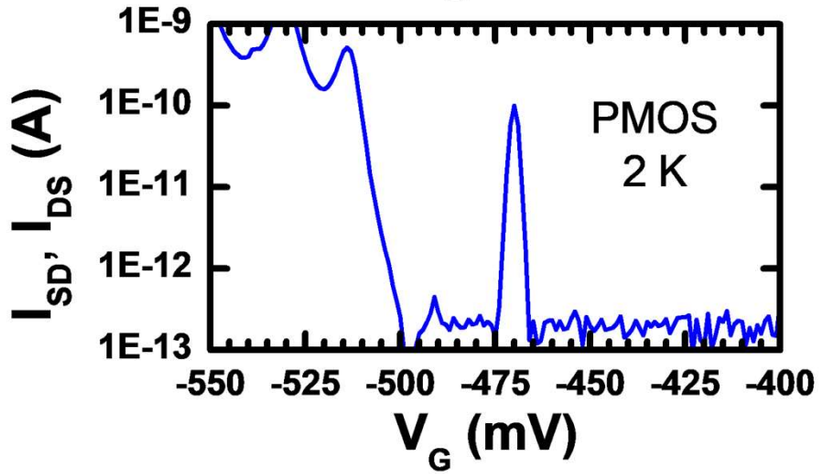



[L. Hutin, ESSDERC 2018]

# Measured MOSFET Transfer Char. : 1x20nmx80nm

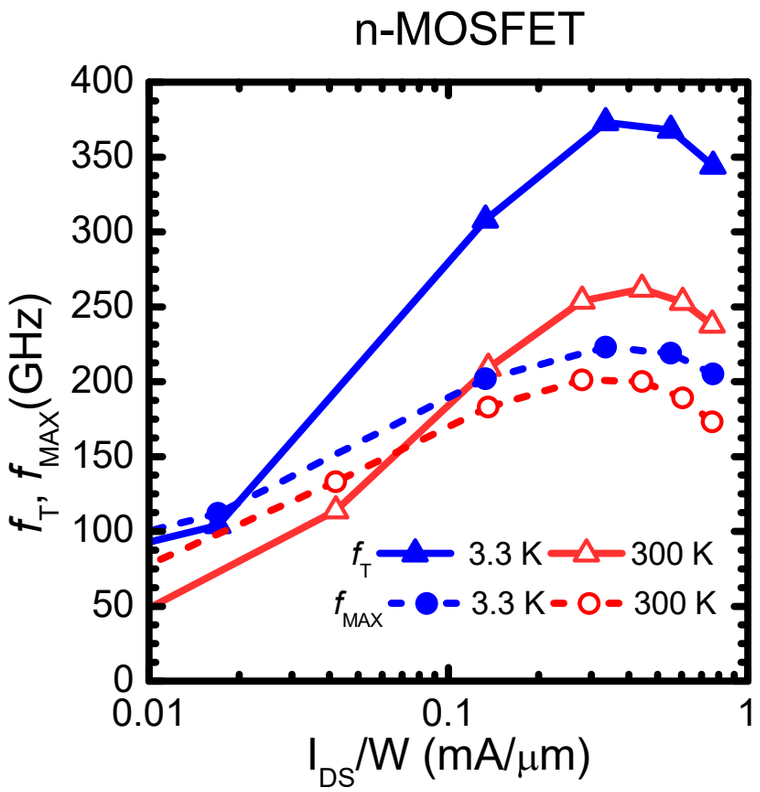


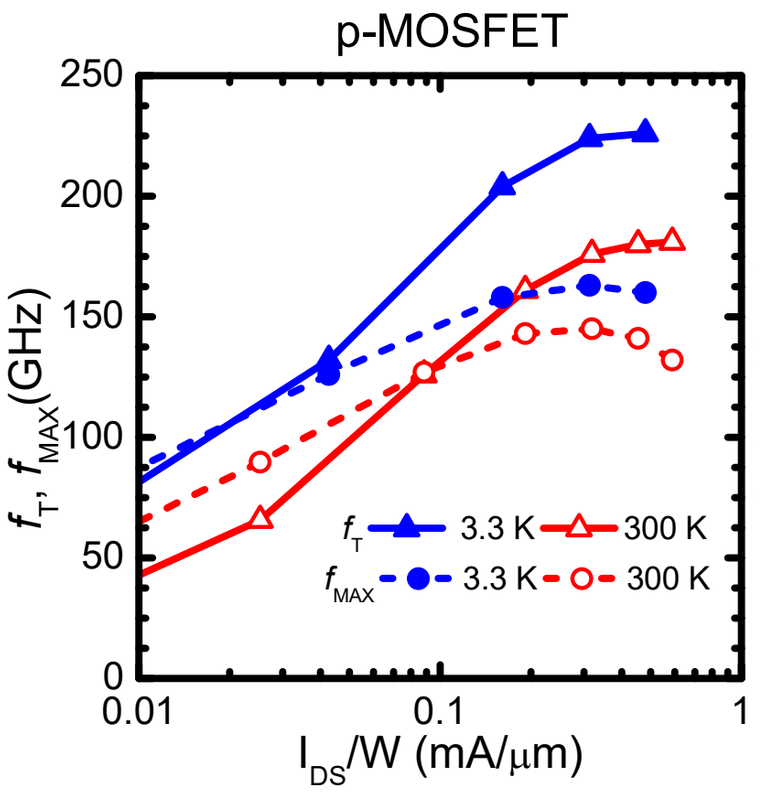



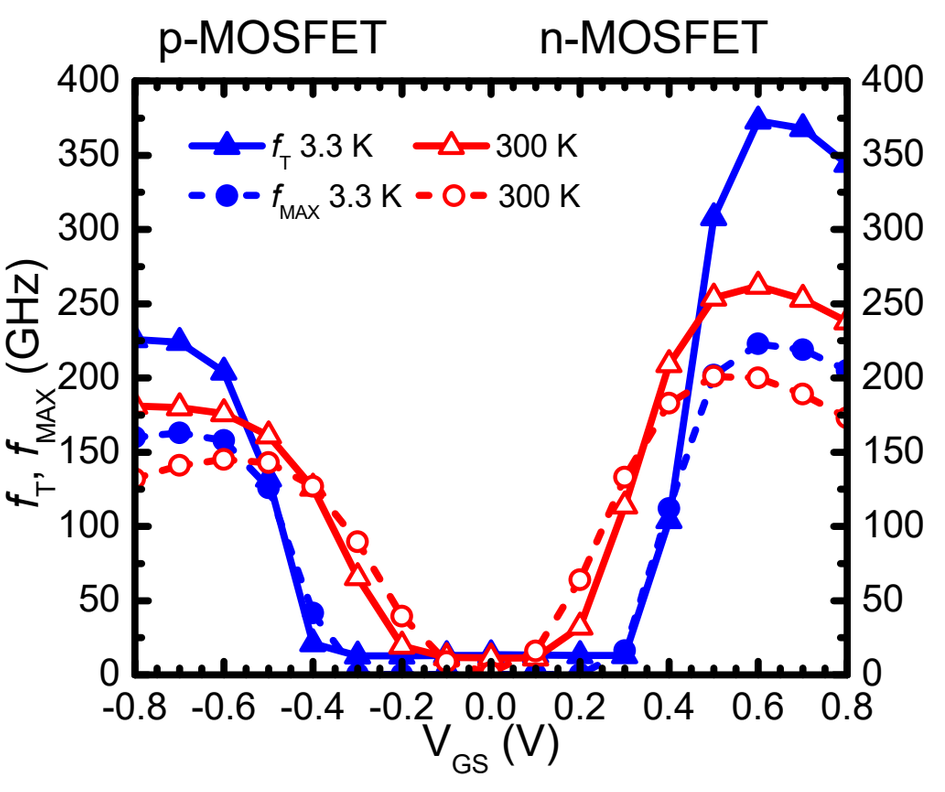




Strong quantum effects in **subthreshold region** at 2 K!

# Measured $f_T$ and $f_{MAX}$: 40x20nmx590nm



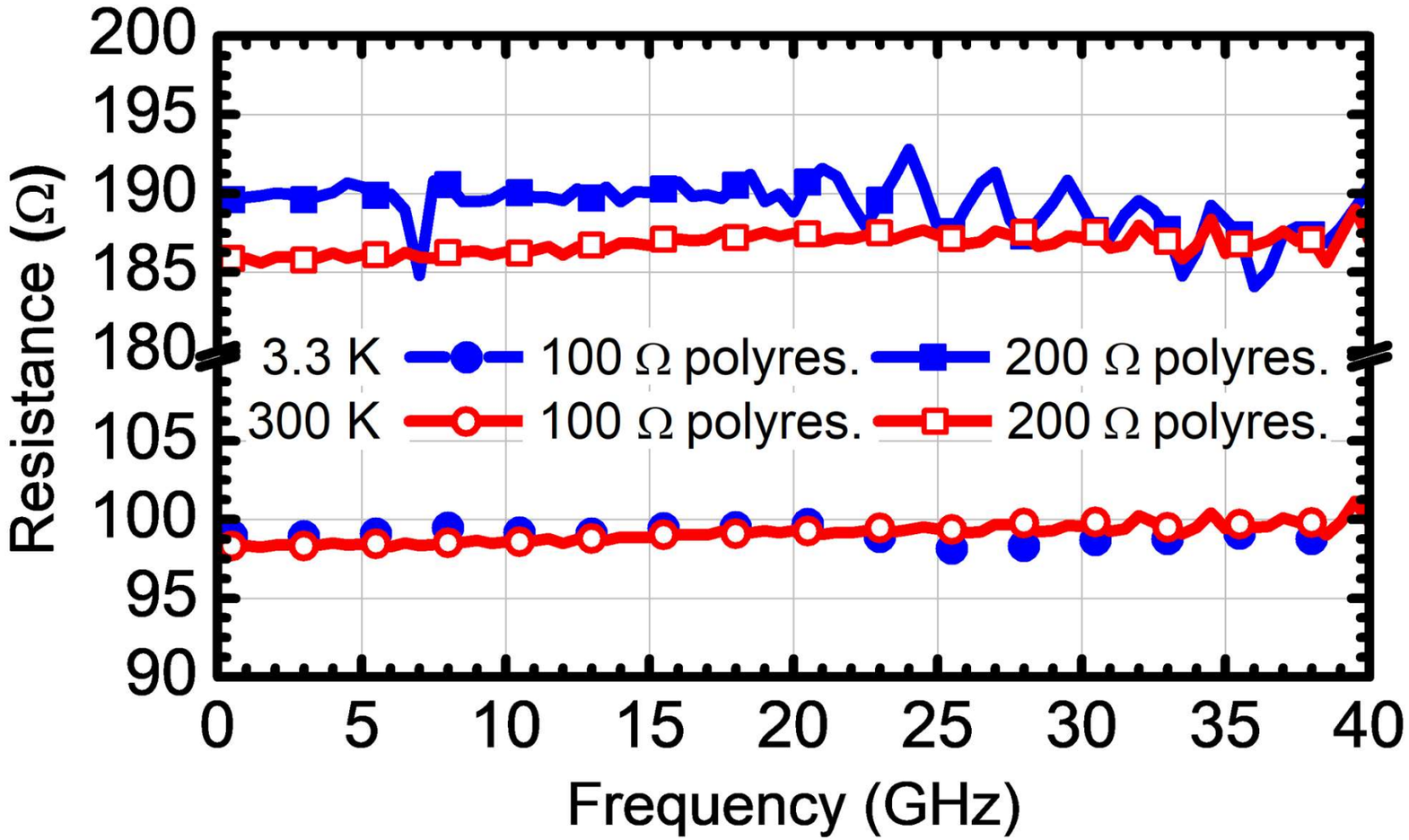




Classical behavior in **saturation region** even at 3.3 K!

- $J_{pf_T}$, $J_{pf_{MAX}}$ invariant over temperature

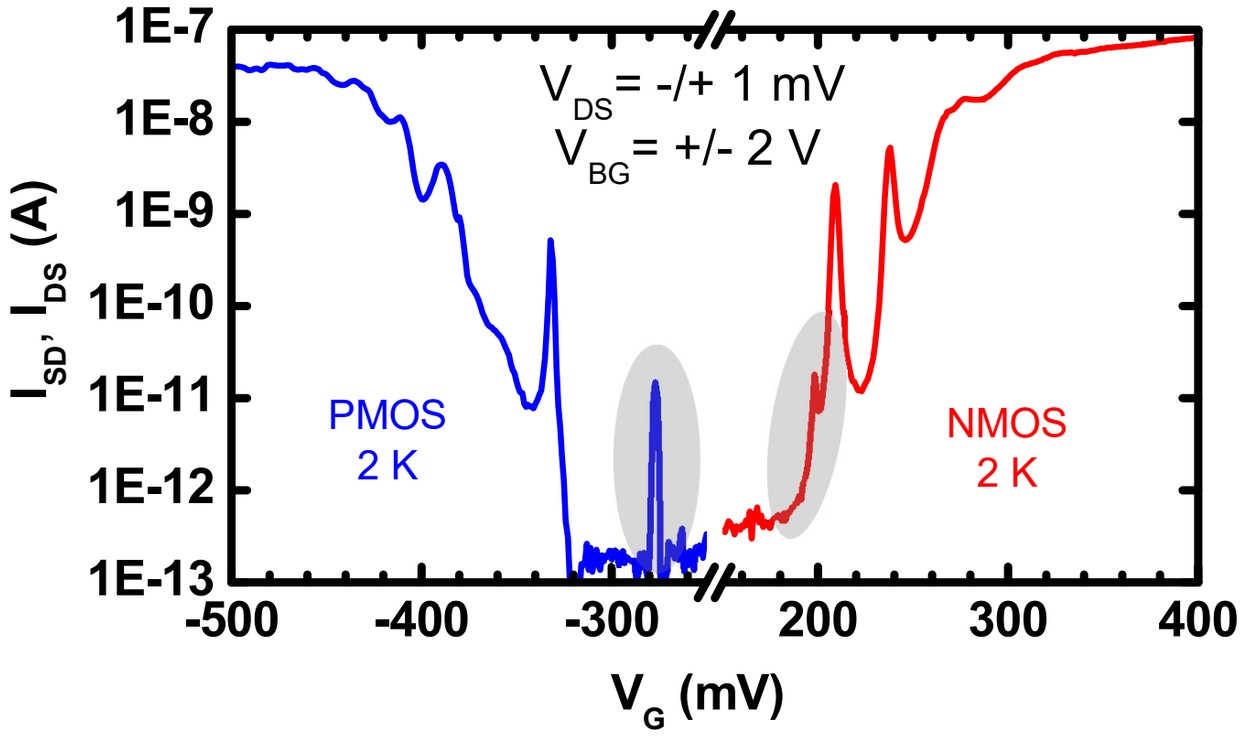
# Measured Poly-Si Resistors vs Temperature



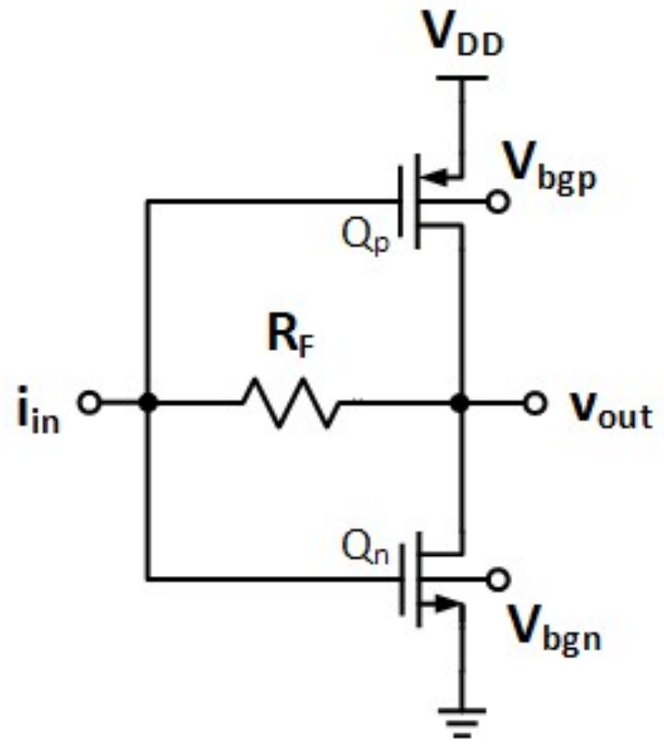

Less than 3% variation over temperature!

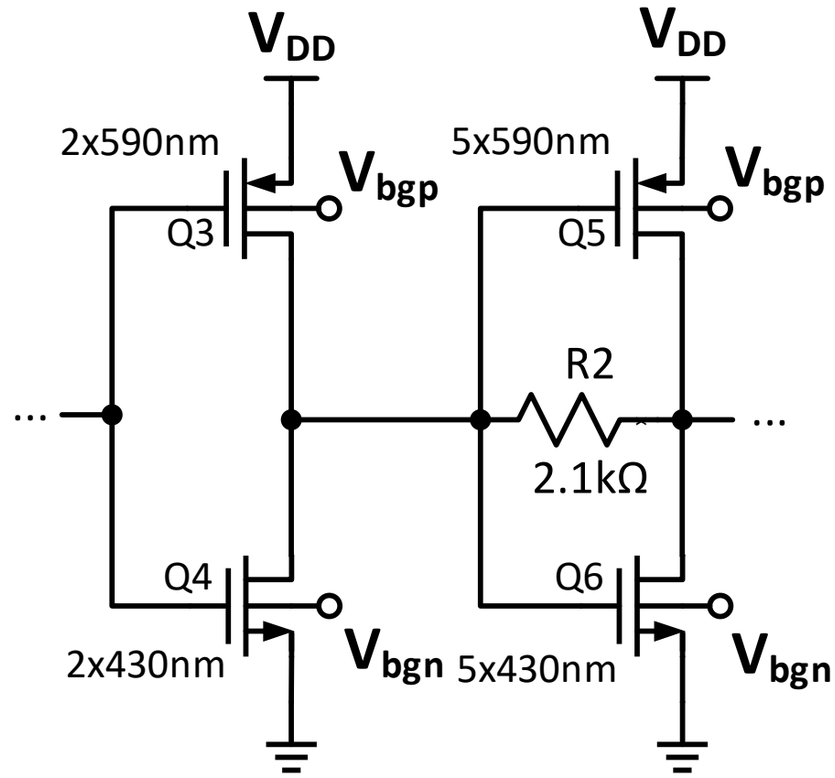
# Readout Amplifier Design Considerations

- Amplify 10pA – 10nA to 1-10 mV
  - $Z_{21}$ =100 – 140 dBΩ
- Lowest possible noise
- BW > $f_{Larmor}/20$ [3]
  - $f_{Larmor} = 60 - 160$ GHz
- $Z_{out}$ = 50 Ω
- $P_{DC}$ < 5 mW



# Amplifier Topology and Design Methodology




- $1 + \frac{W_p}{W_n}$ times less power
- $J_{pfMAX} = 0.25\ \mathrm{mA/\mu m}$

- INV+TIA = Cherry Hooper stage
- Fanout < 3 to maximize BW

# Low Noise TIA Design

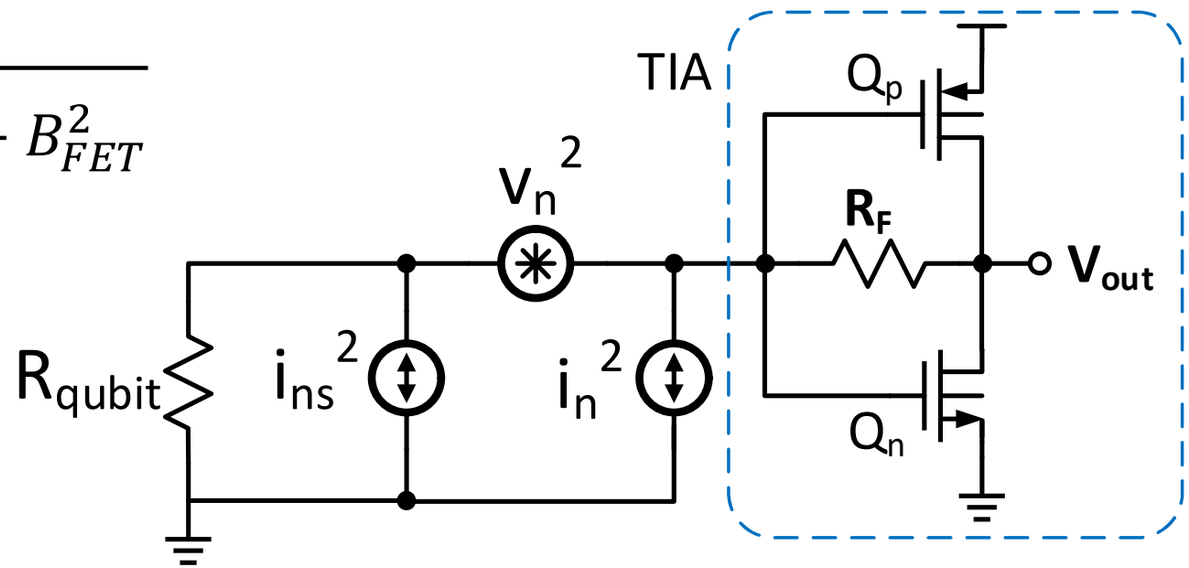
$R_{FET}, G_{FET}, G_{C,FET}, B_{C,FET}$ = technology noise parameters at $J_{opt}$

→ dependent on $g_m, R_s, R_g, C_{gs}, C_{gd}$

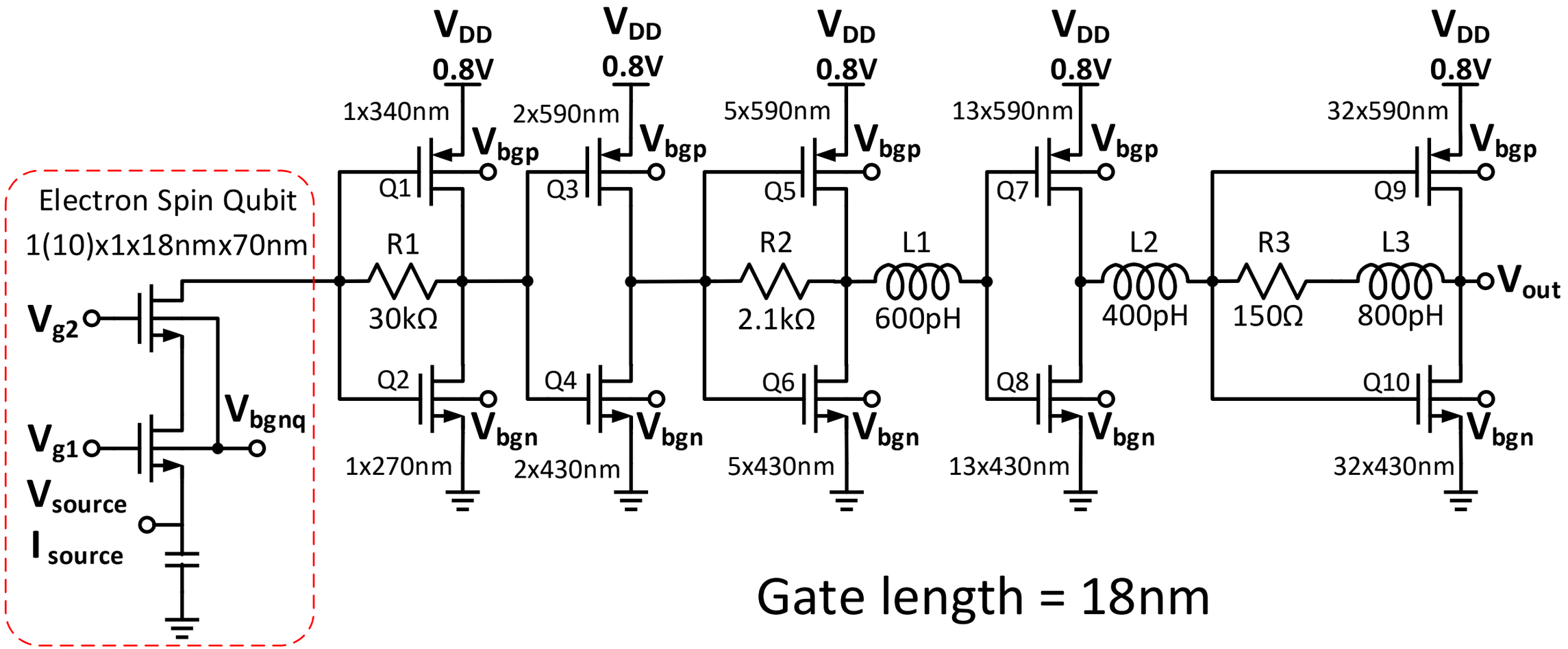
$$W_{opt} = \frac{1}{\omega}\left(\frac{1}{\mathrm{R_{qubit}}} + \frac{1}{\mathrm{R_F}}\right)\sqrt{\frac{1}{\frac{G_{FET}}{R_{FET}} + G_{C,FET}^2 + B_{FET}^2}}$$

$W_{opt,n} = 0.271\ \mu m, W_{opt,p} = 0.339\ \mu m$

@ 19 GHz, $\mathrm{R_{qubit}} = 50\ \mathrm{k\Omega}, \mathrm{R_F} = 30\ \mathrm{k\Omega}$

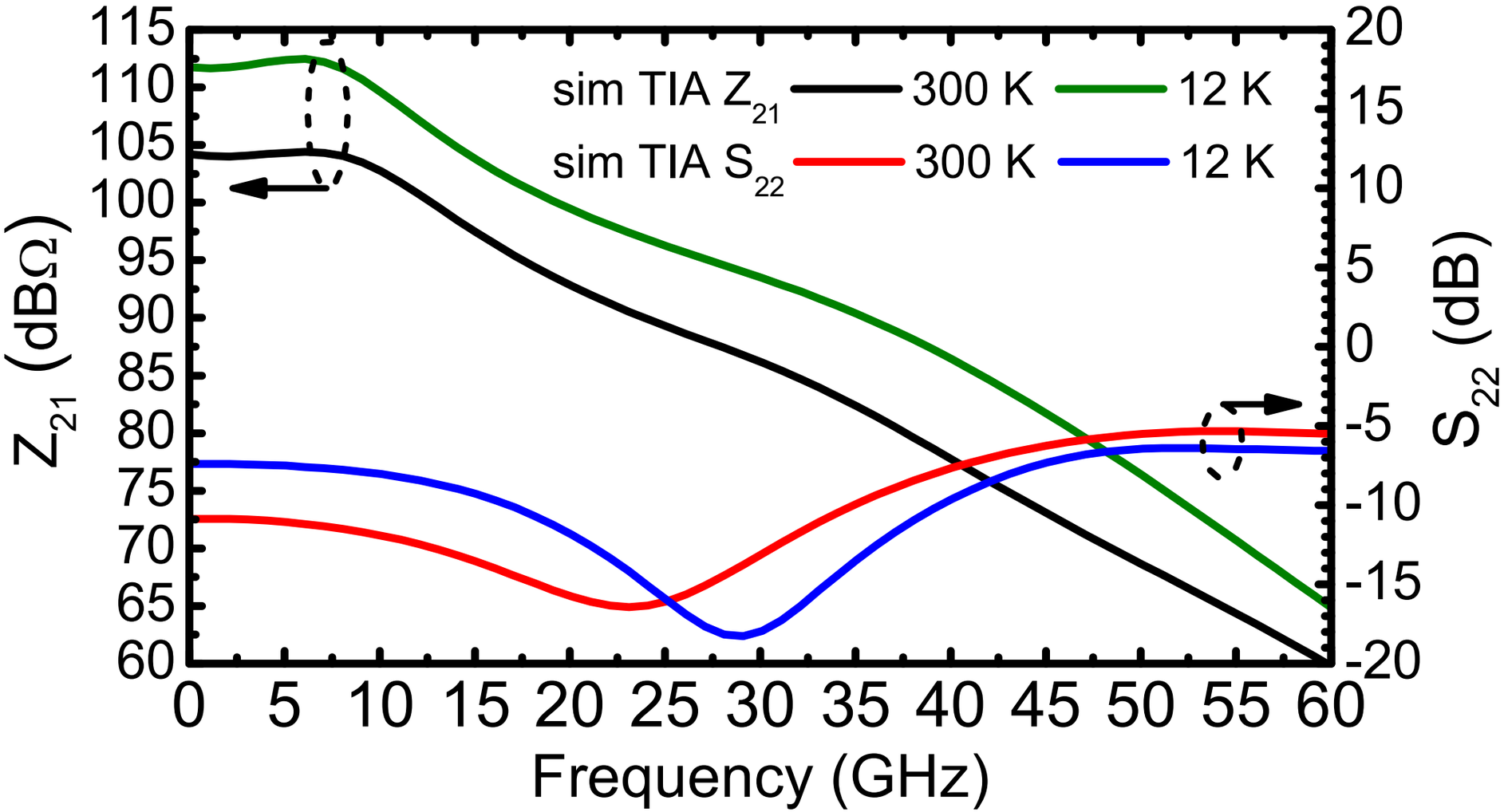


# Double Quantum Dot (DQD) with Readout Amplifier

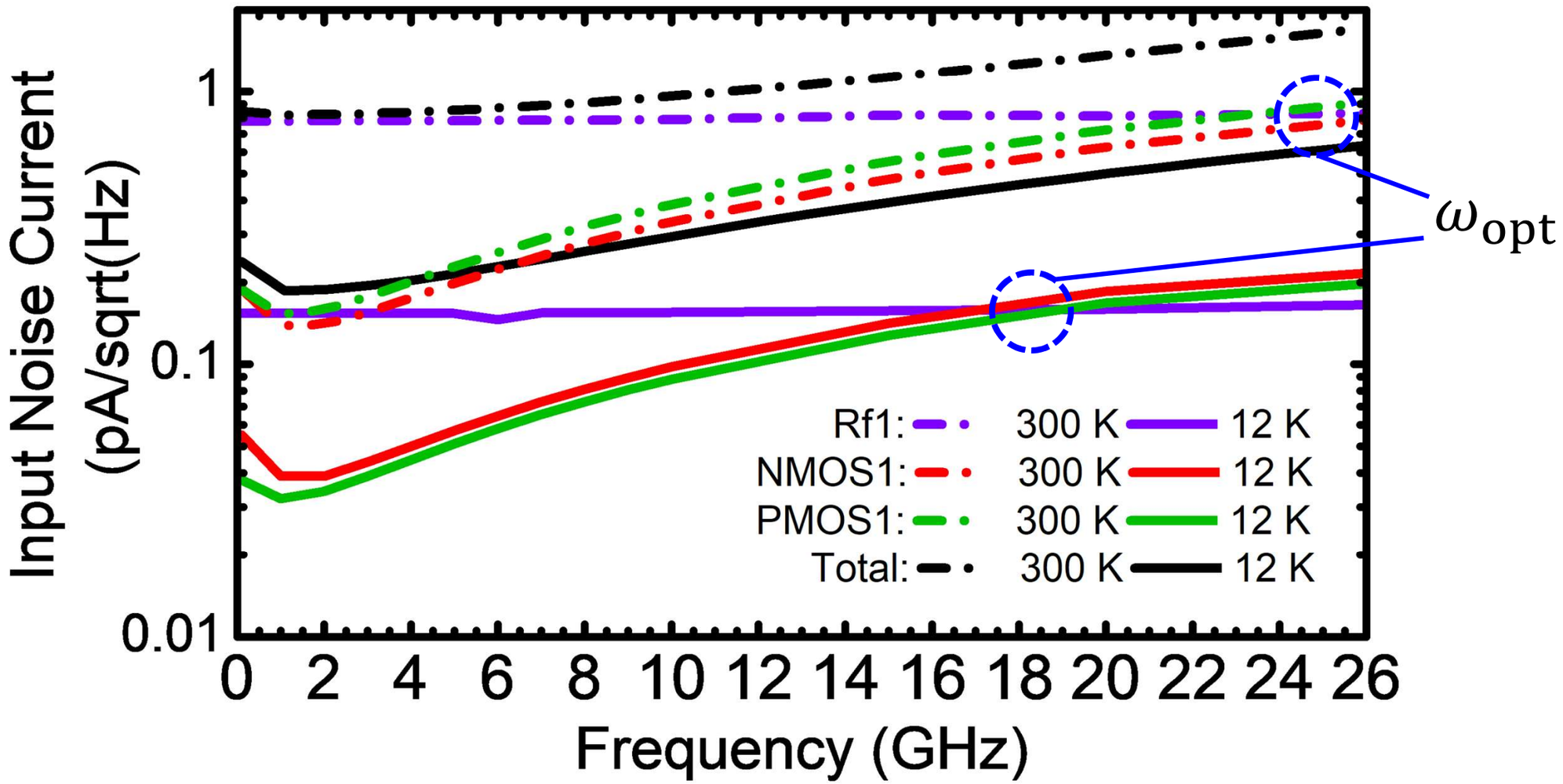



Gate length = 18nm

# Simulated 5-stage TIA S-parameters



# Simulated 5-stage TIA Noise Contributions



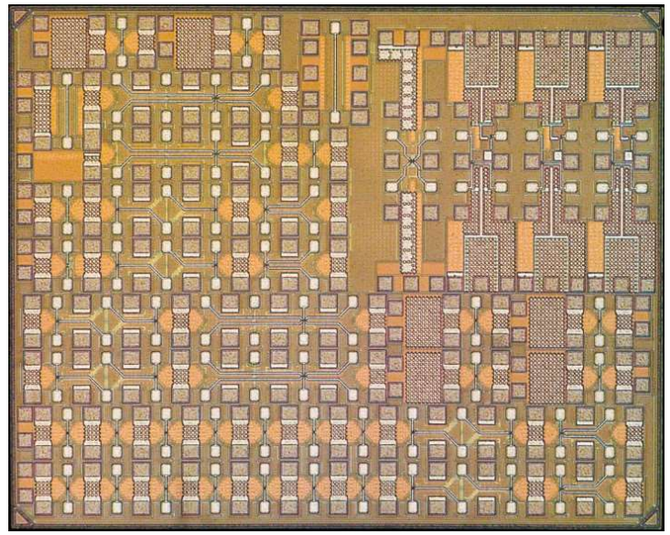
# Fabrication: 22nm FDSOI CMOS

2 tapeouts: 10M and 11M BEOL

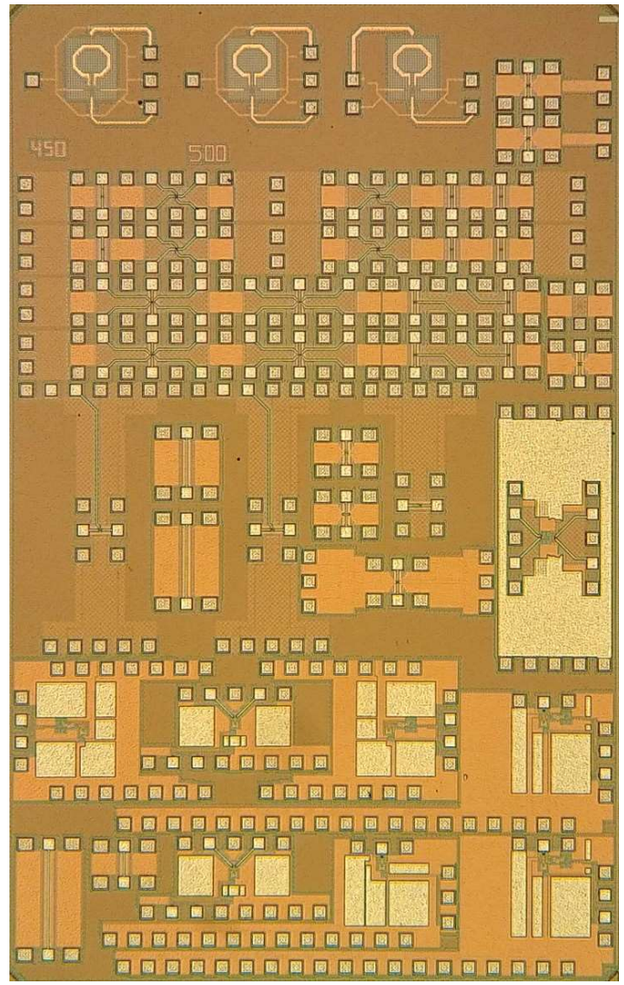
Measurements conducted at:

1. Lake Shore Cryotronics @ 2 K
2. U of Waterloo @ 3.3 K
3. IMT Bucharest @ 5 K- 300 K
4. U of Toronto @ 300 K

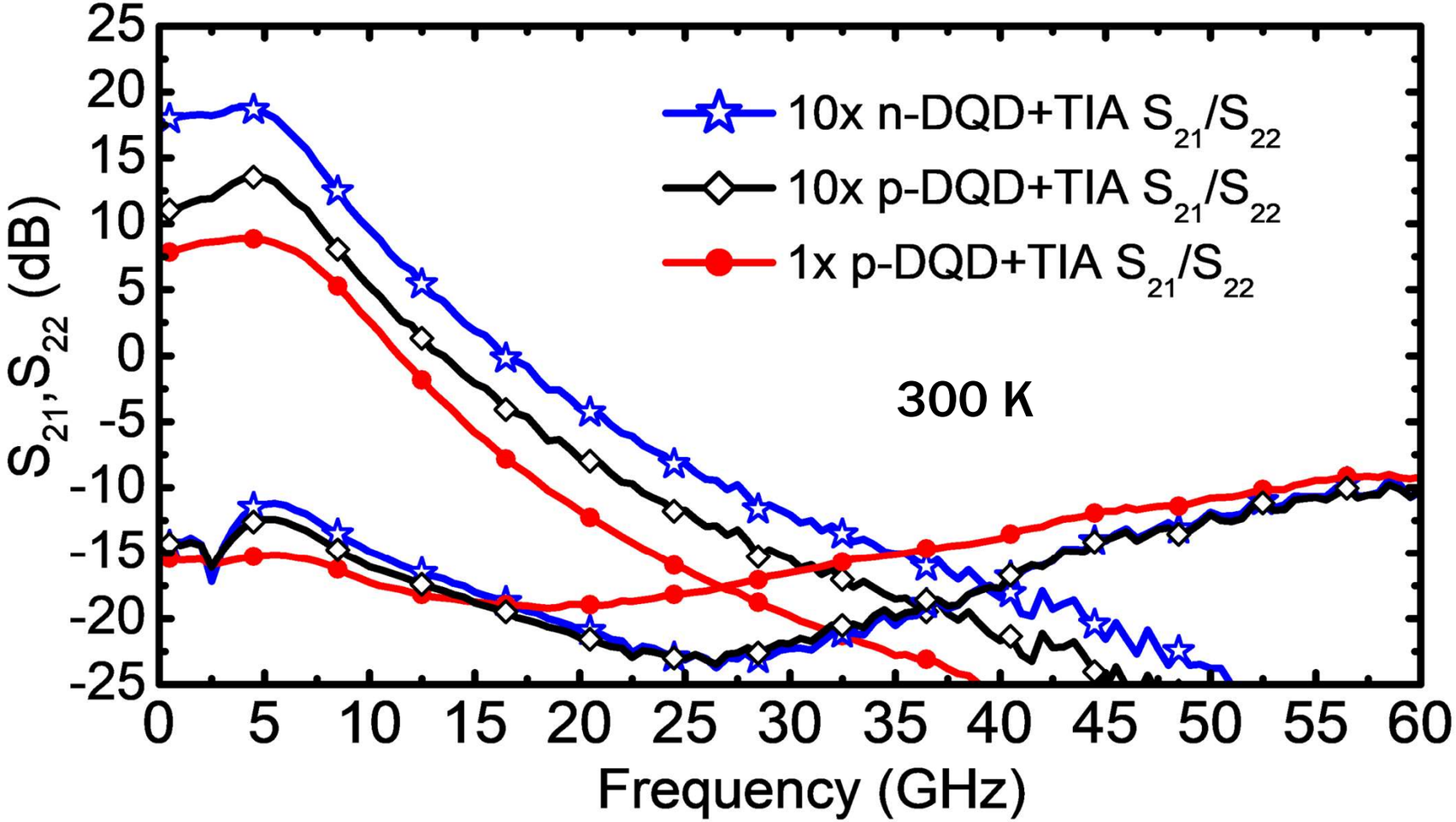
2.5mm x 2.0mm



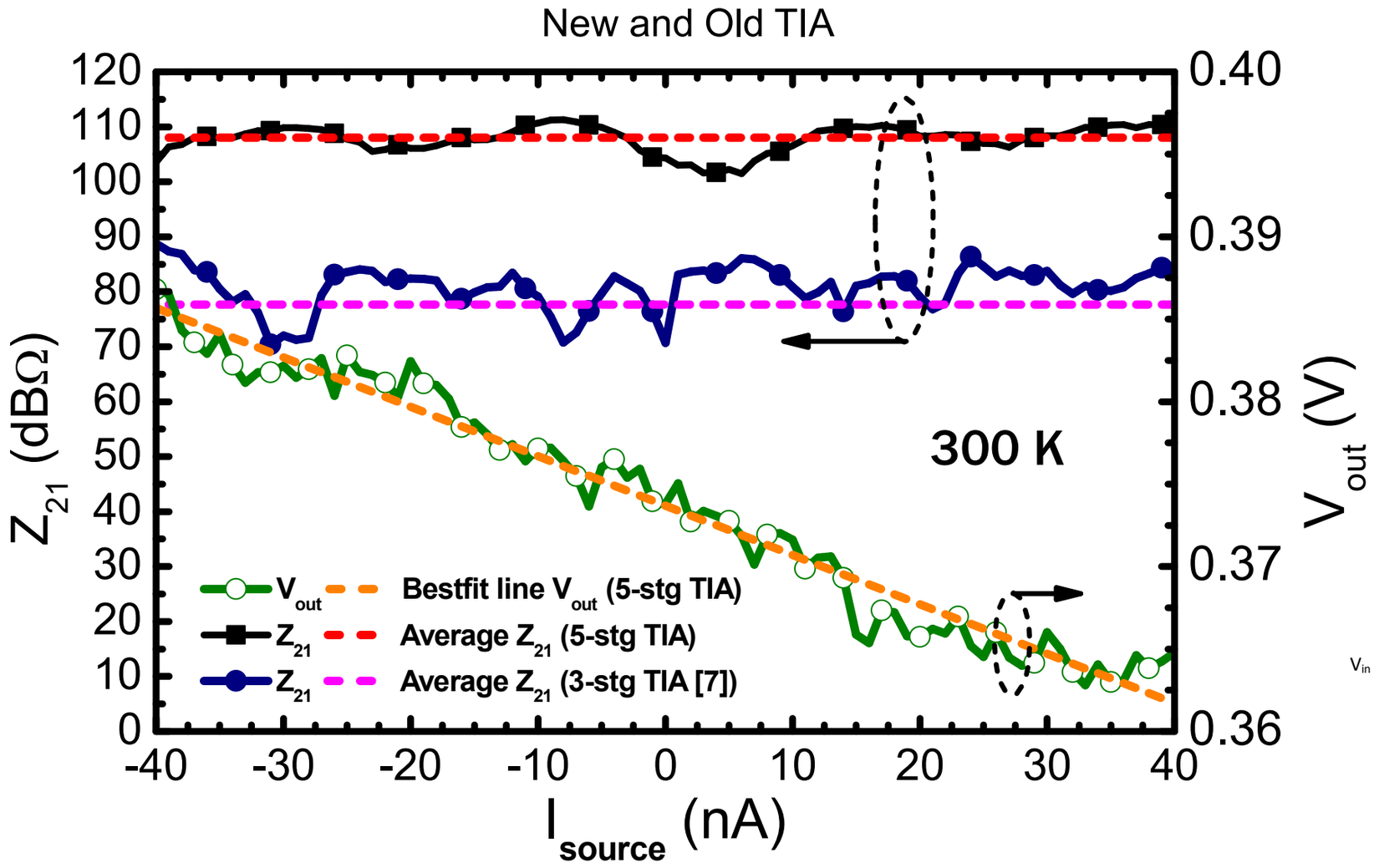
2.5mm x 4.0mm

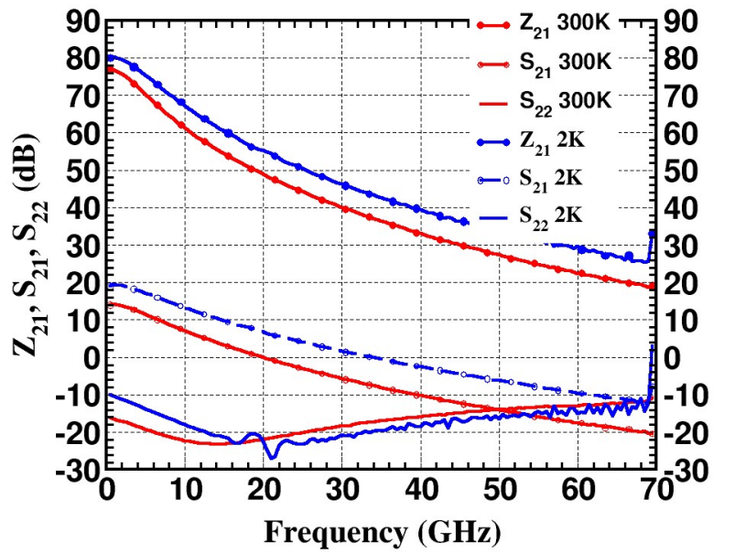


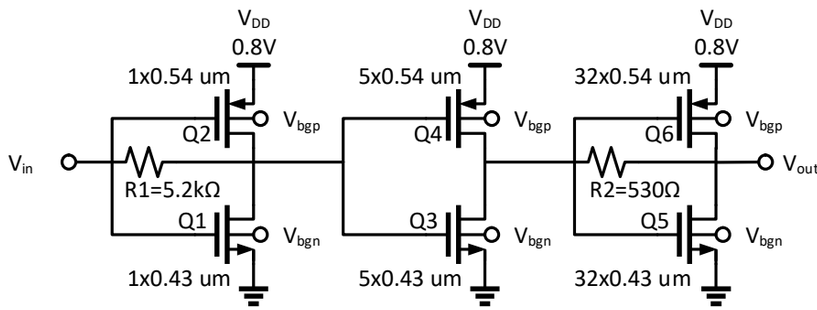
# Measured S-params. of DQD+TIA Circuits



# Measured New and Old Readout Amplifiers

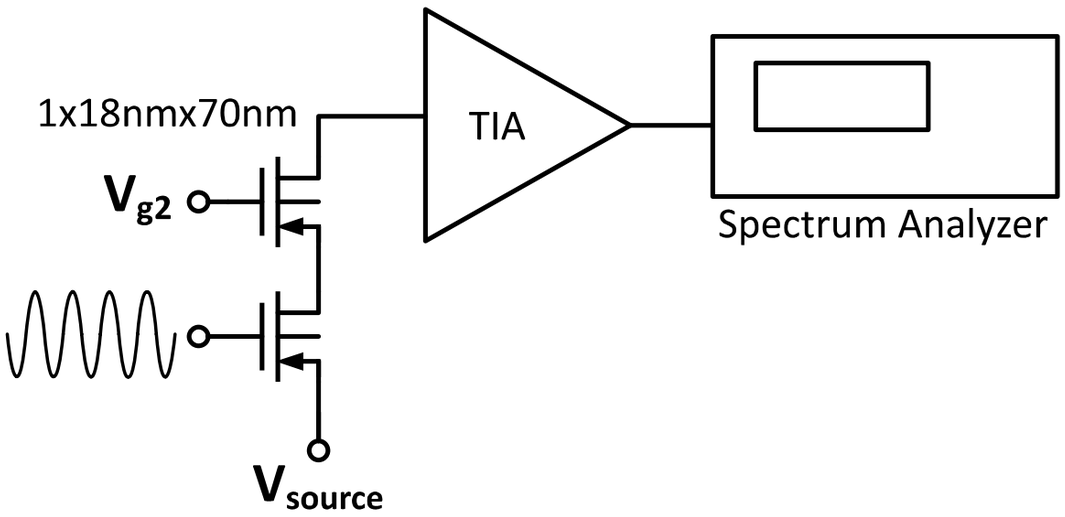


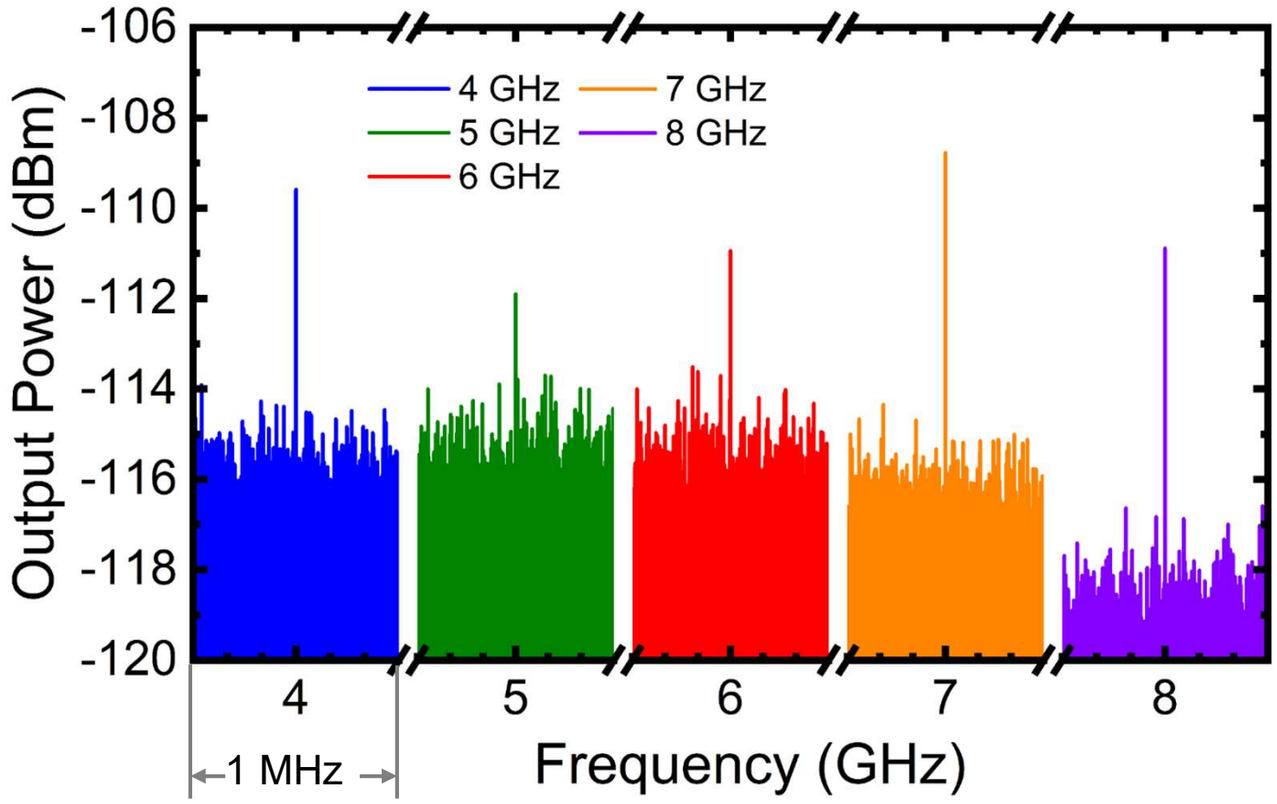




[S. Bonen, EDL 2019]

# Meas. 300K Output Spectrum of 1x p-DQD+TIA for Sinusoidal Inputs




$v_{in} = 3.2\ \mu V_p, f_{in} = 4$ GHz

$P_{out}$ = -109 dBm, SNR = 6 dB

$\rightarrow$ $I_{in} = 3\ pA_{rms}$ ($Z_{21} = 108$ dBΩ)

RBW = 1 Hz

# Conclusion

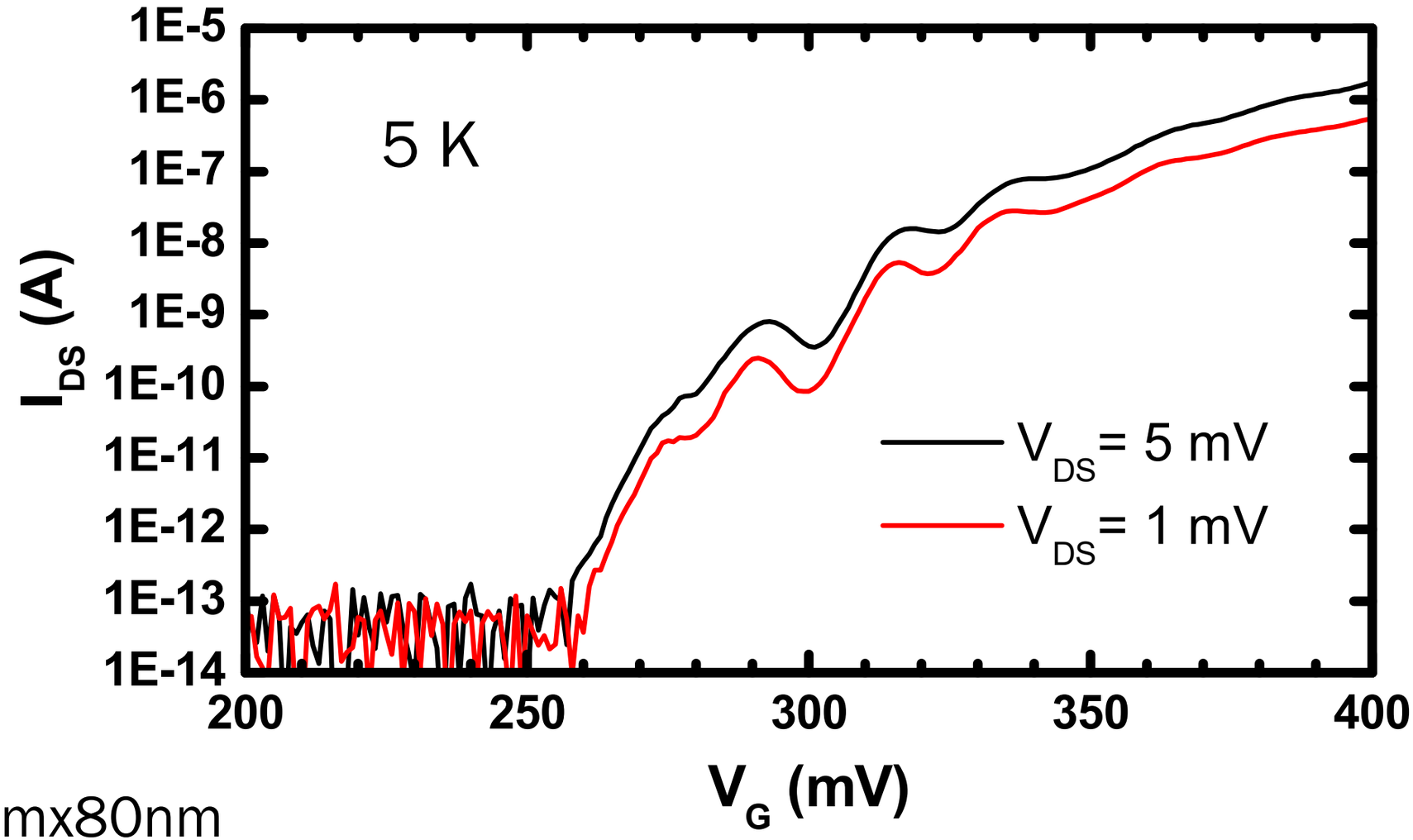
- Monolithic qubit+TIA readout in a production 22nm FDSOI CMOS
- Minimum-sized transistors, cascodes used as single, double QDs
- $f_T, f_{MAX}$ improve at 2 K while $J_{pf_T}, J_{pf_{MAX}}$ remain same as 300 K
- Unique TIA topology with 108 dBΩ gain, 12 GHz BW and < 1 pA/$\sqrt{Hz}$ input noise current at 300 K
- Cryogenic IC design possible with 300 K models

# Acknowledgement


- NSERC for funding
- Globalfoundries for chip fabrication and donation
- Dr. Nigel Cave for technology discussions
- Lakeshore and Keysight for testing
- Integrand for EMX
- Jaro Pristupa for CAD support
- CMC for CAD Tools

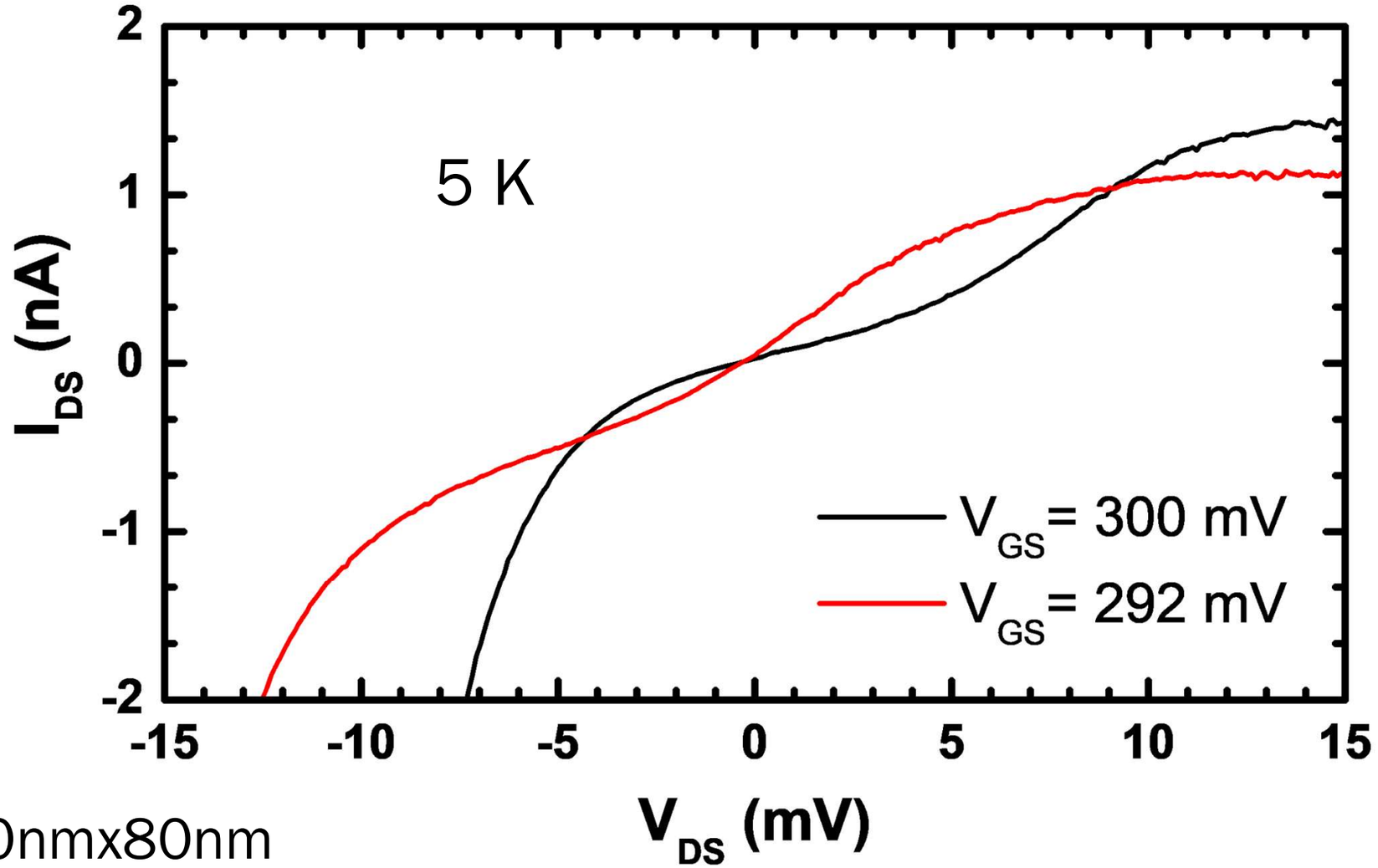
# BACKUP SLIDES

# Measured n-MOSFET Transfer Characteristics



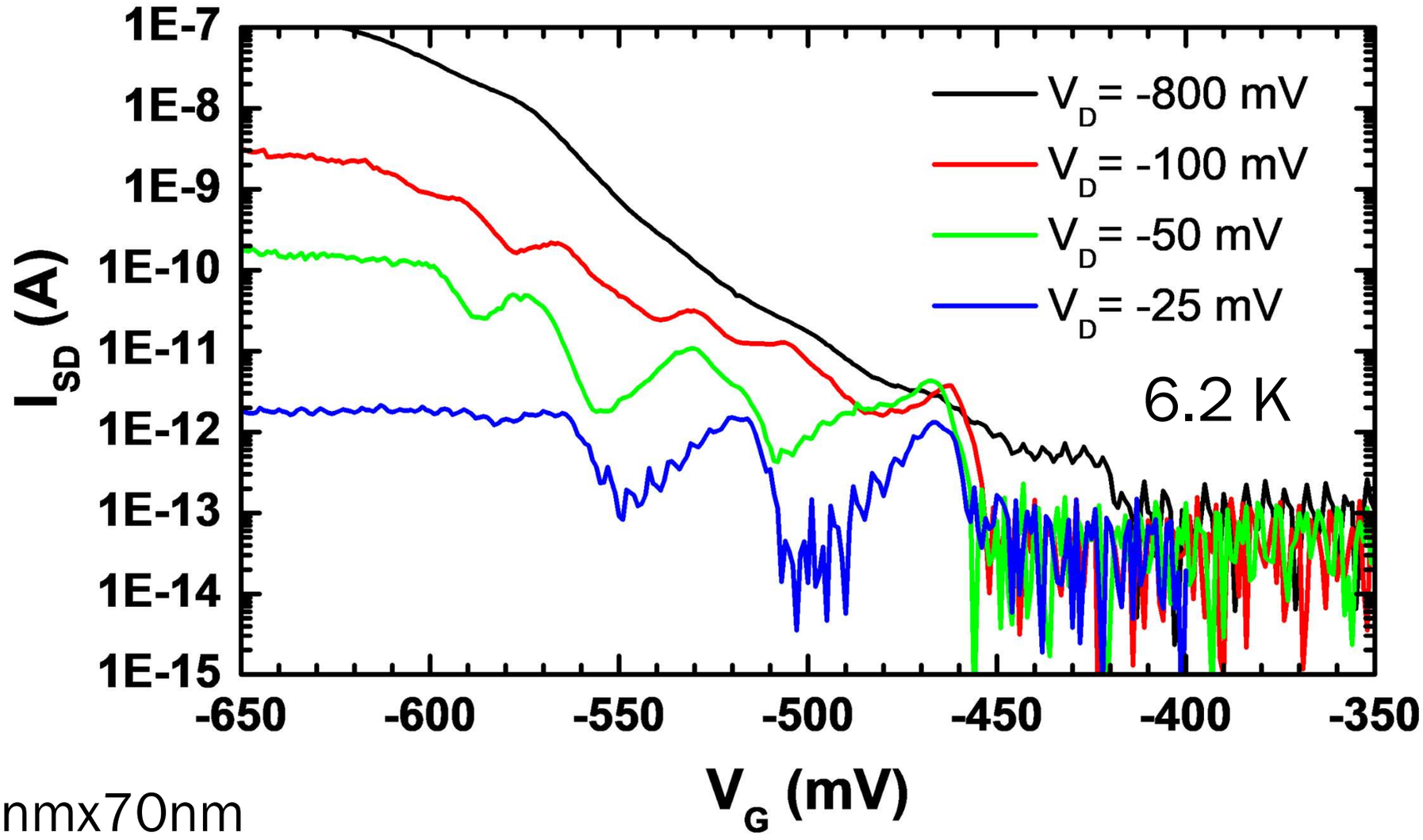

40x20nmx80nm

# Measured n-MOSFET Output Characteristics



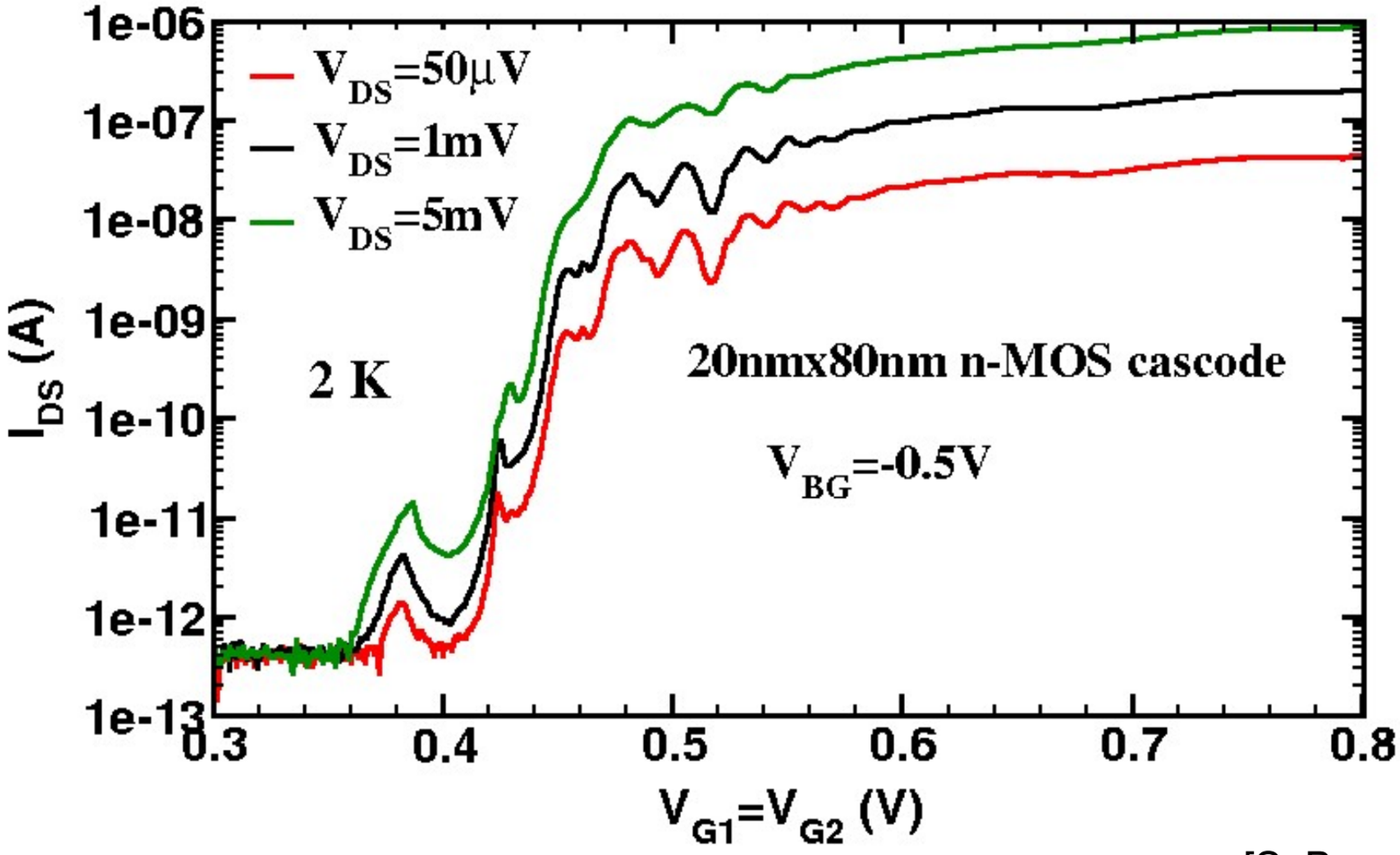

40x20nmx80nm

# Measured p-MOSFET Transfer Characteristics



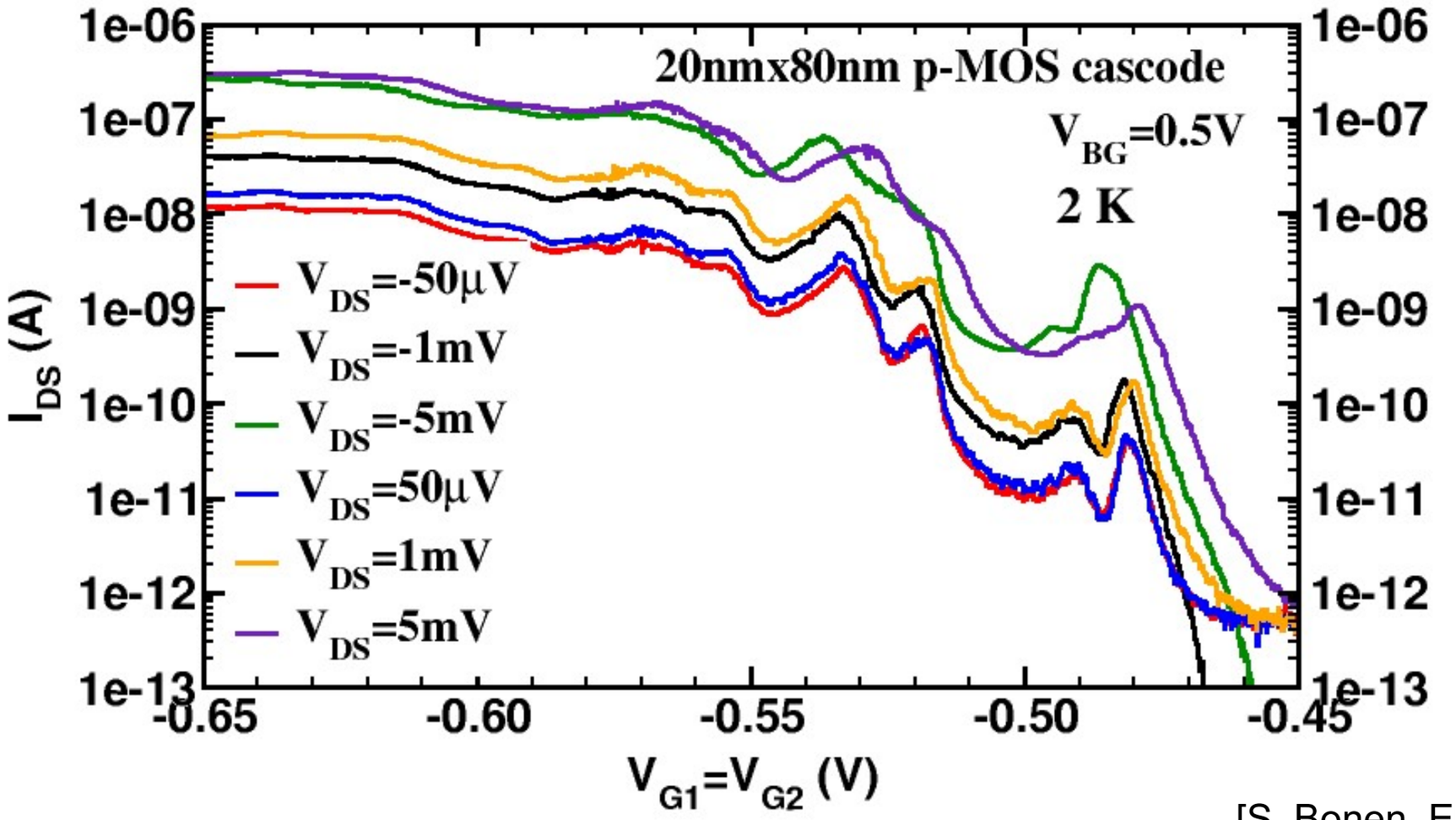

1x18nmx70nm

# Measured n-MOSFET Cascode Transfer Characteristics




[S. Bonen, EDL 2019]

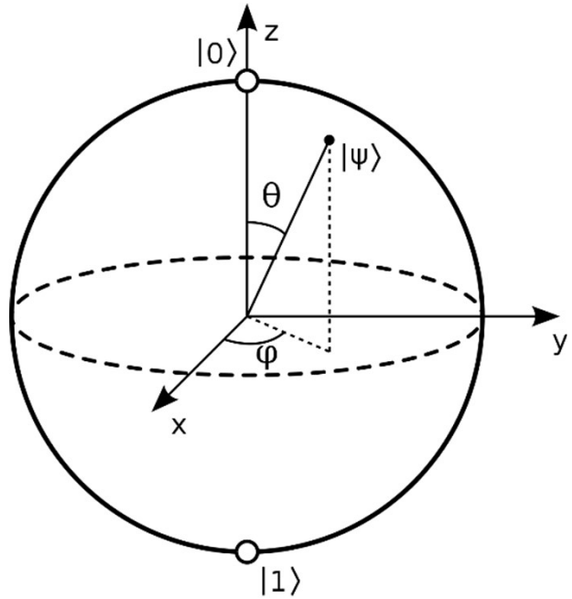
# Measured p-MOSFET Cascode Transfer Characteristics

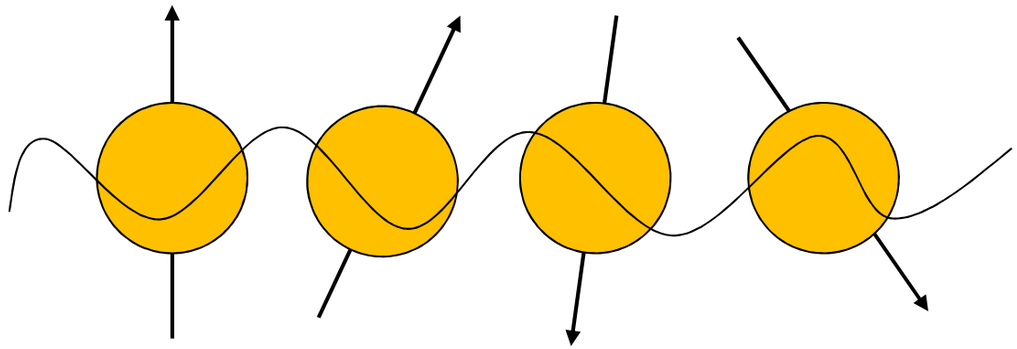



[S. Bonen, EDL 2019]

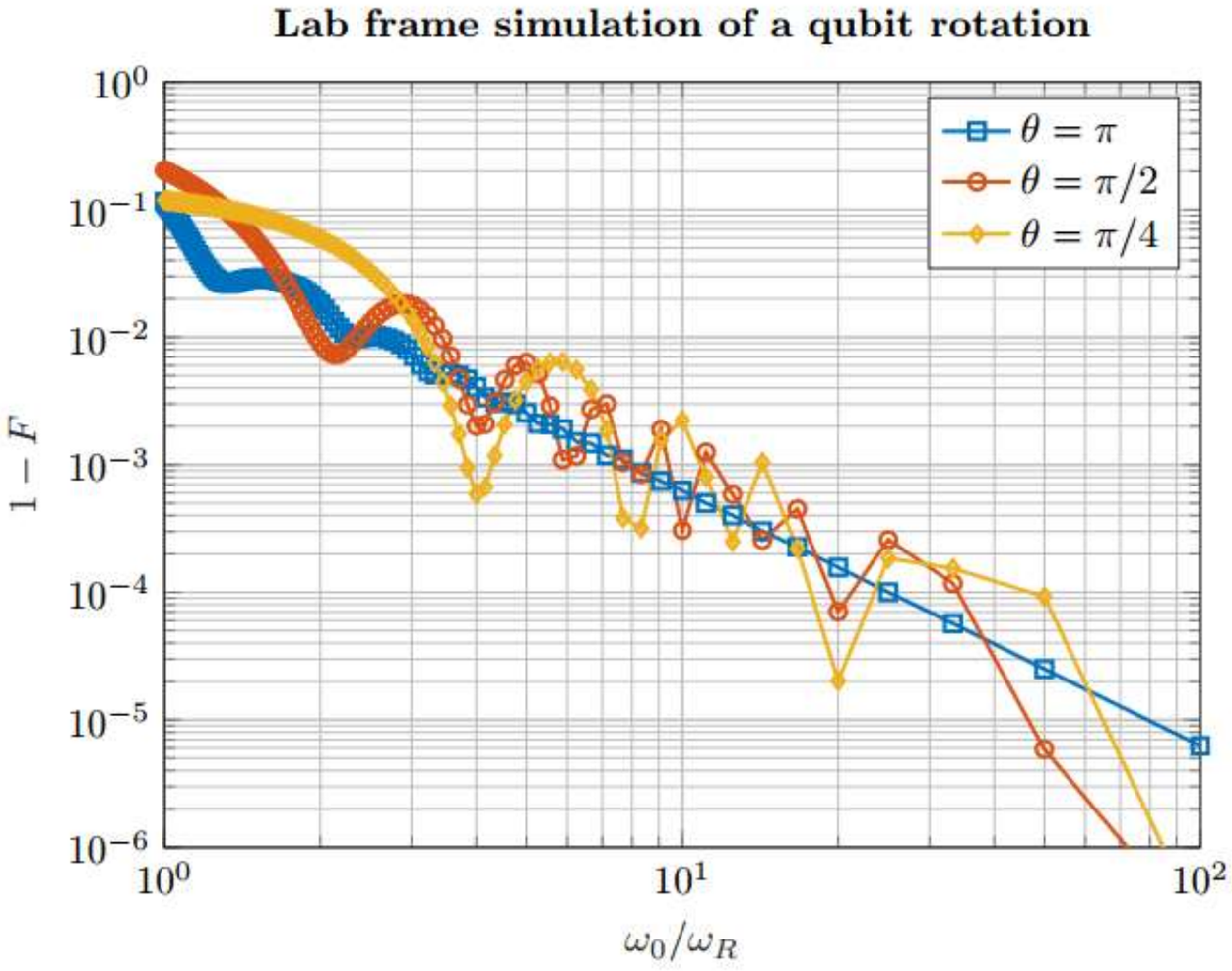
# What is a Qubit?

- Unit of quantum information
  - States $|0\rangle$ or $|1\rangle$
  - $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$
- Superposition + Entanglement
- ‘n’ - entangled qubits form a Quantum Circuit



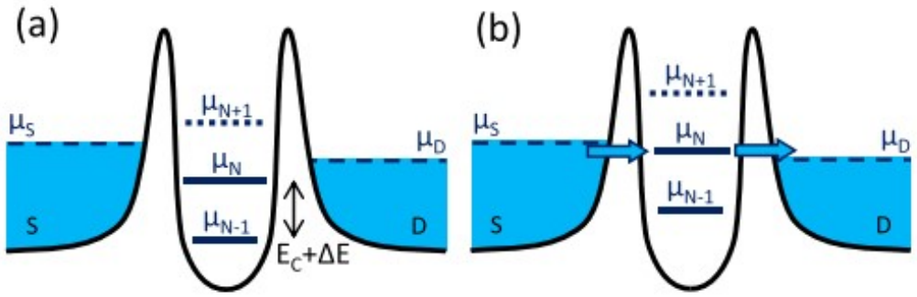



# Qubit Fidelity vs Larmor to Rabi Frequency Ratio

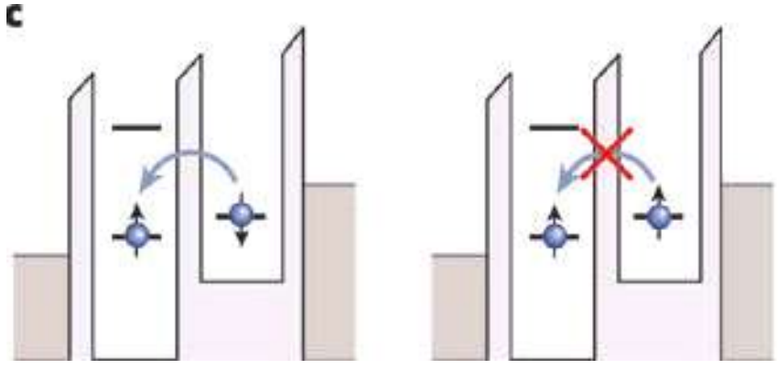



[J.P.G. van Dijk, arxiv 2018]

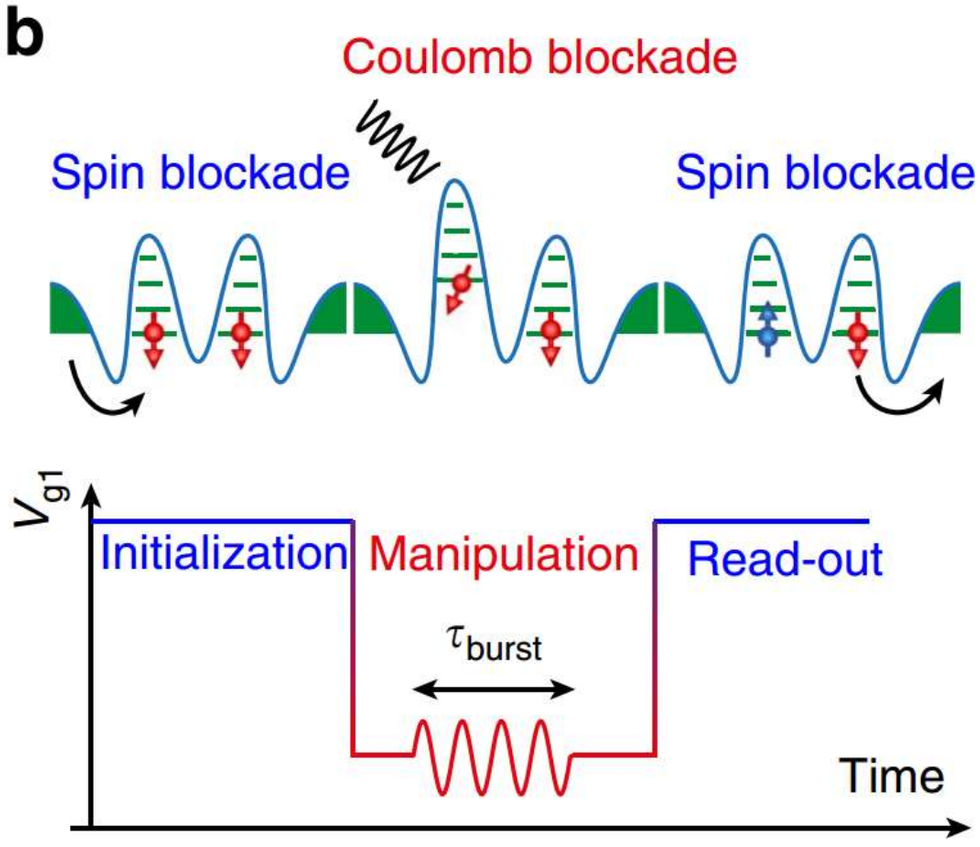
# Qubit Readout with Double Quantum Dot




Coulomb Blockade [F.Zwanenburg, 2013]

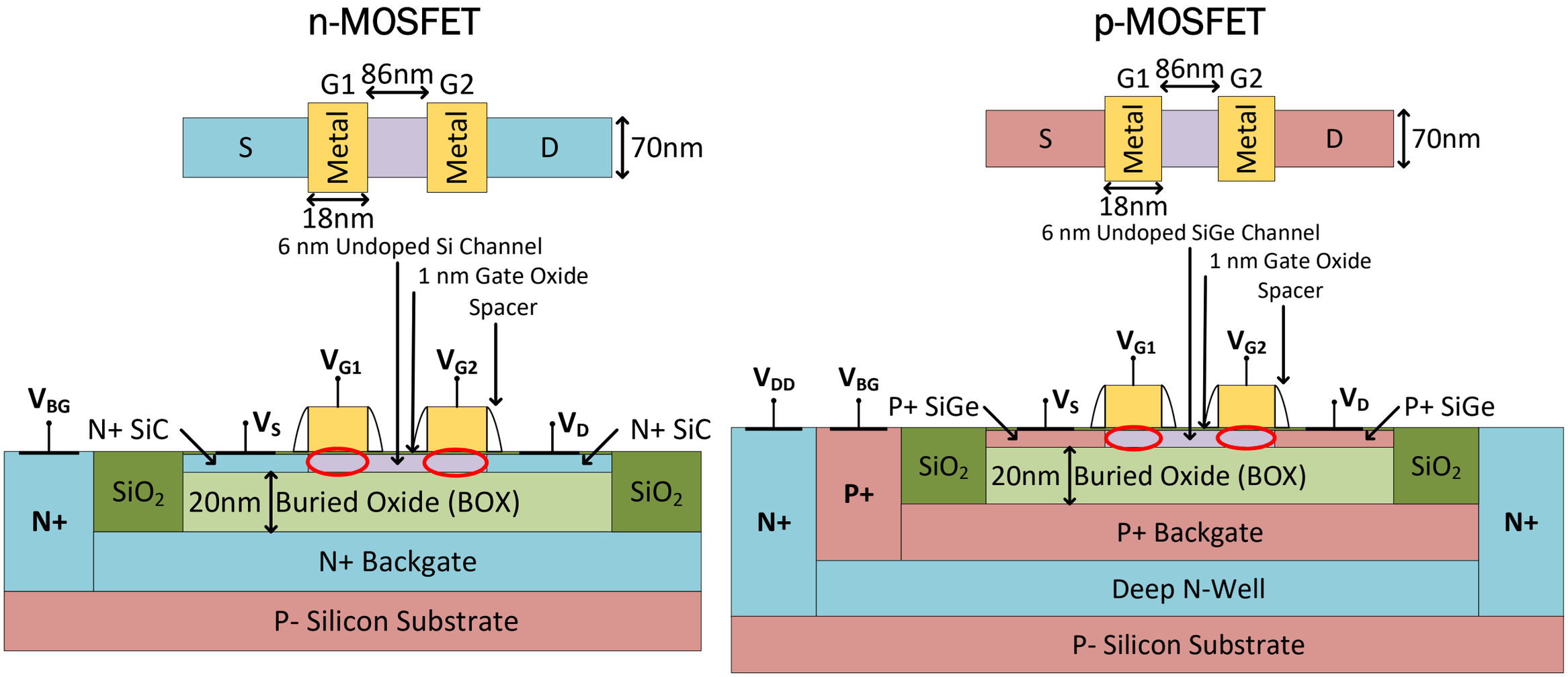



Pauli Spin Blockade [R.Hanson, Nature 2008]

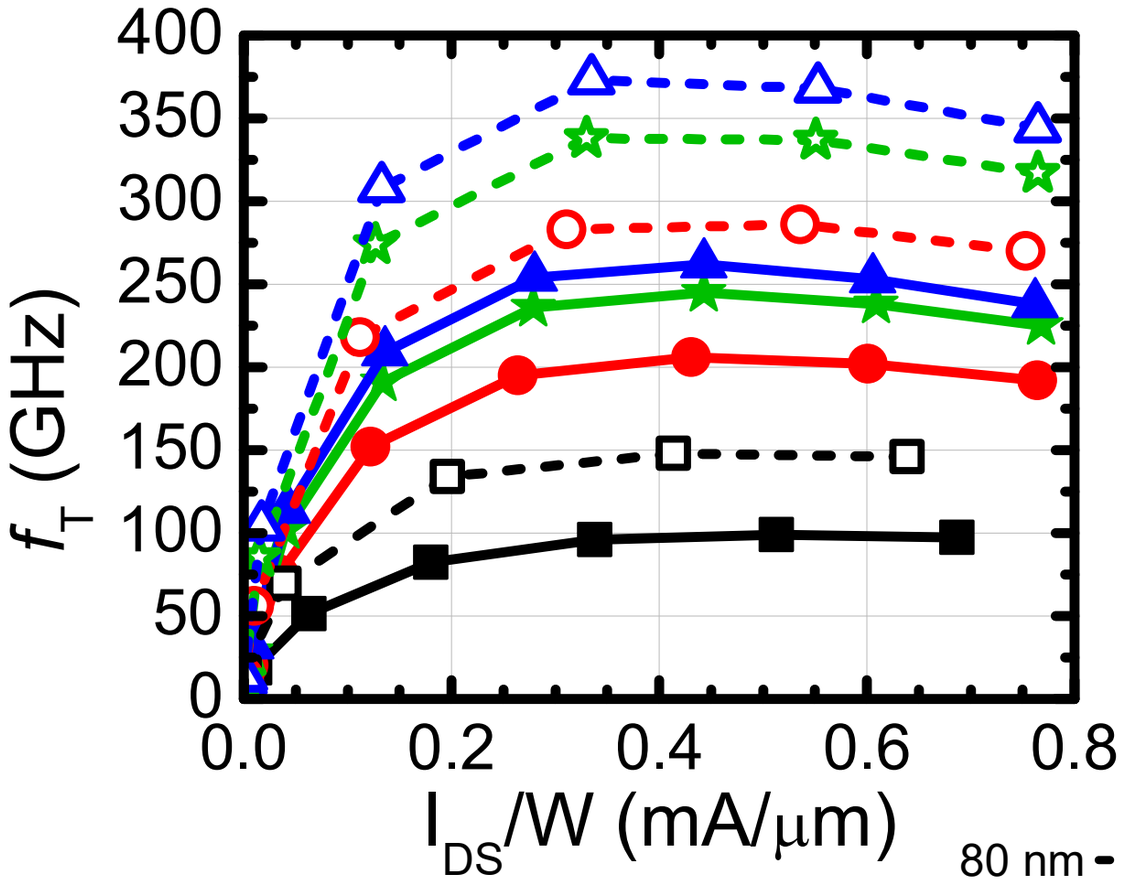


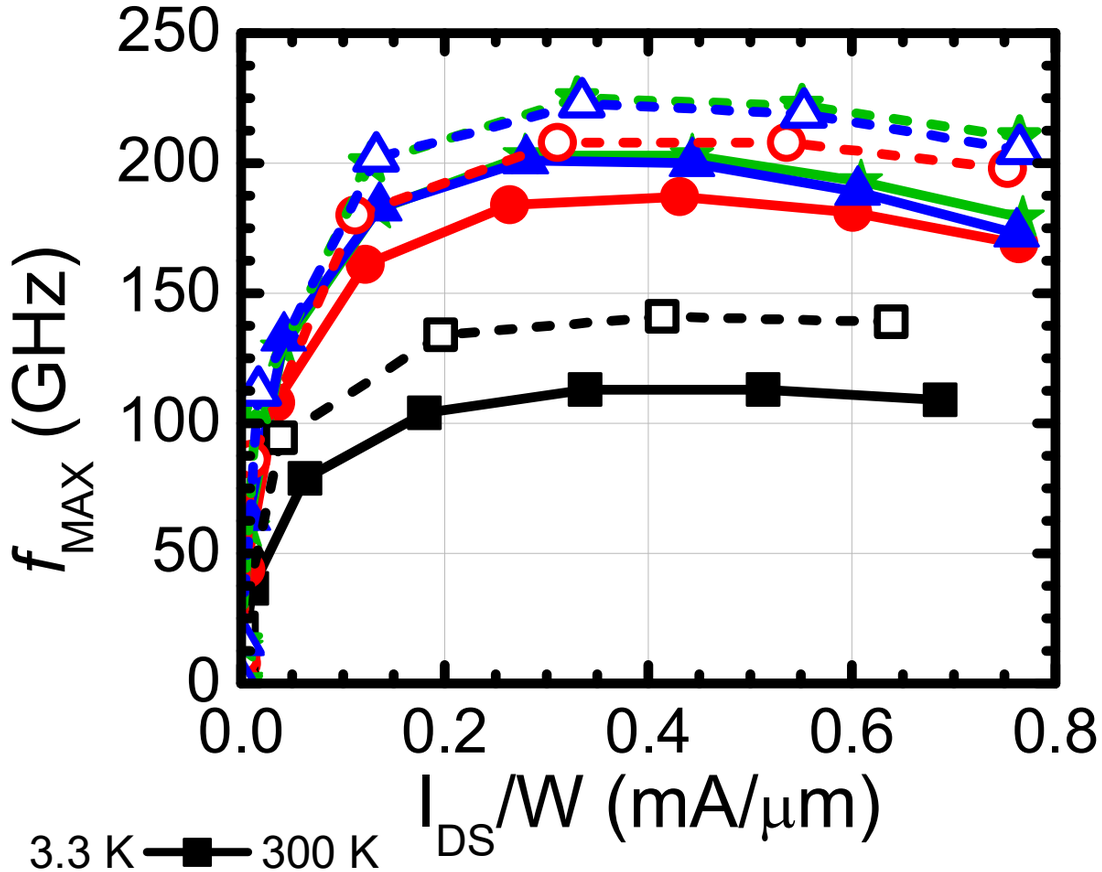

[R. Maurand, Nature 2016]

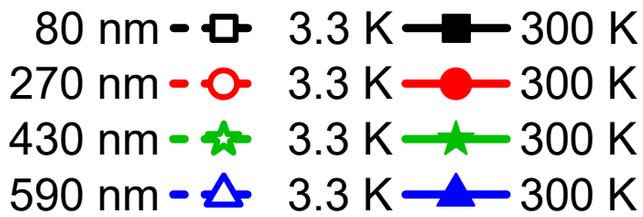
# Complementary QDs in 22nm FDSOI CMOS



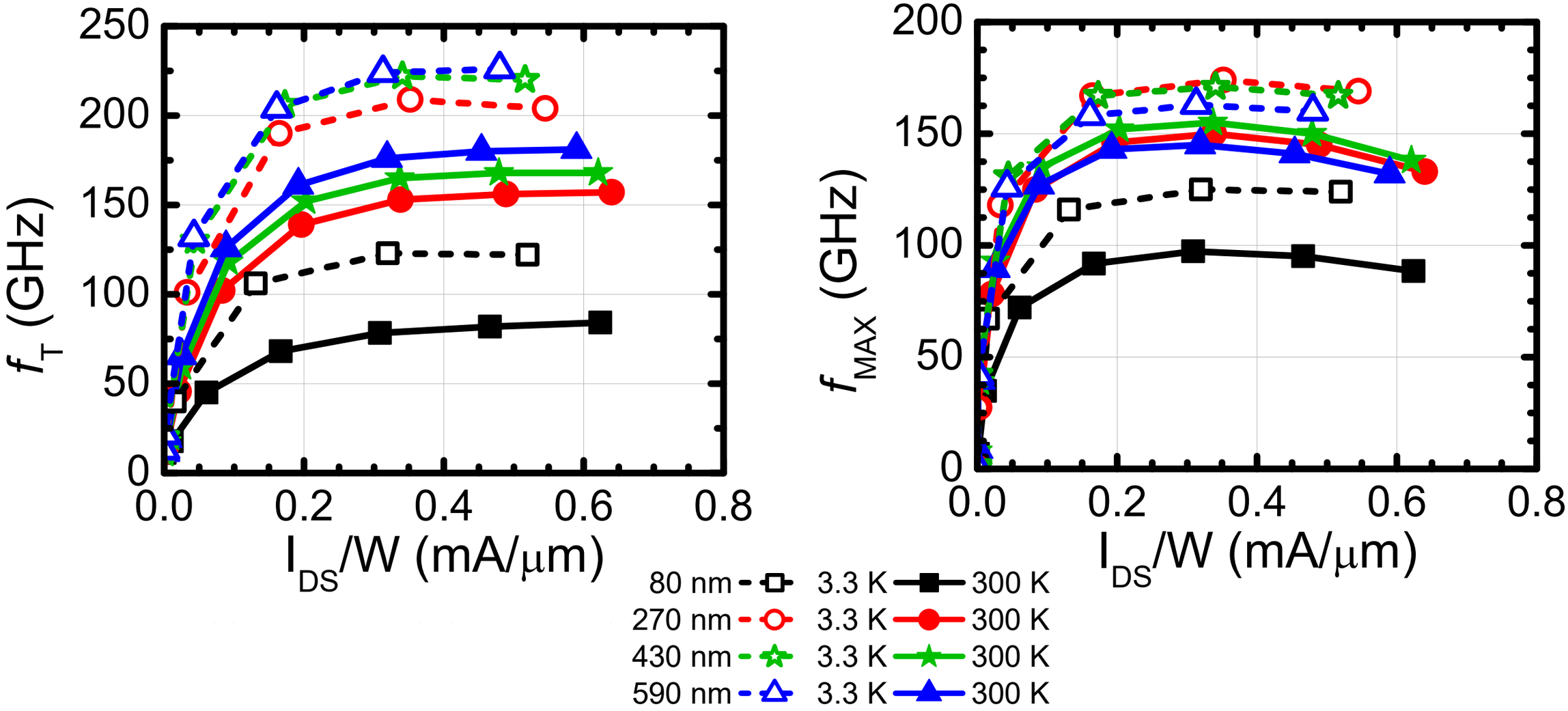
# Measured n-MOSFET $f_T, f_{MAX}$ vs. $W_f$



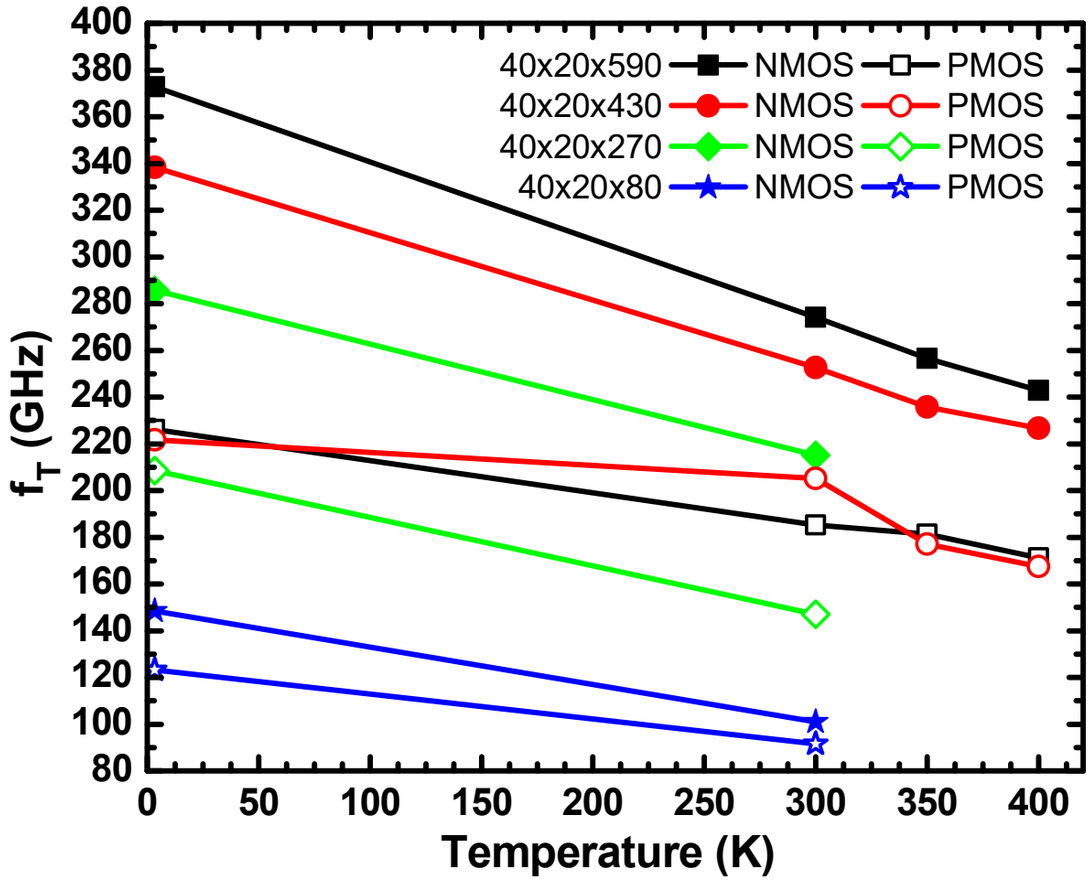



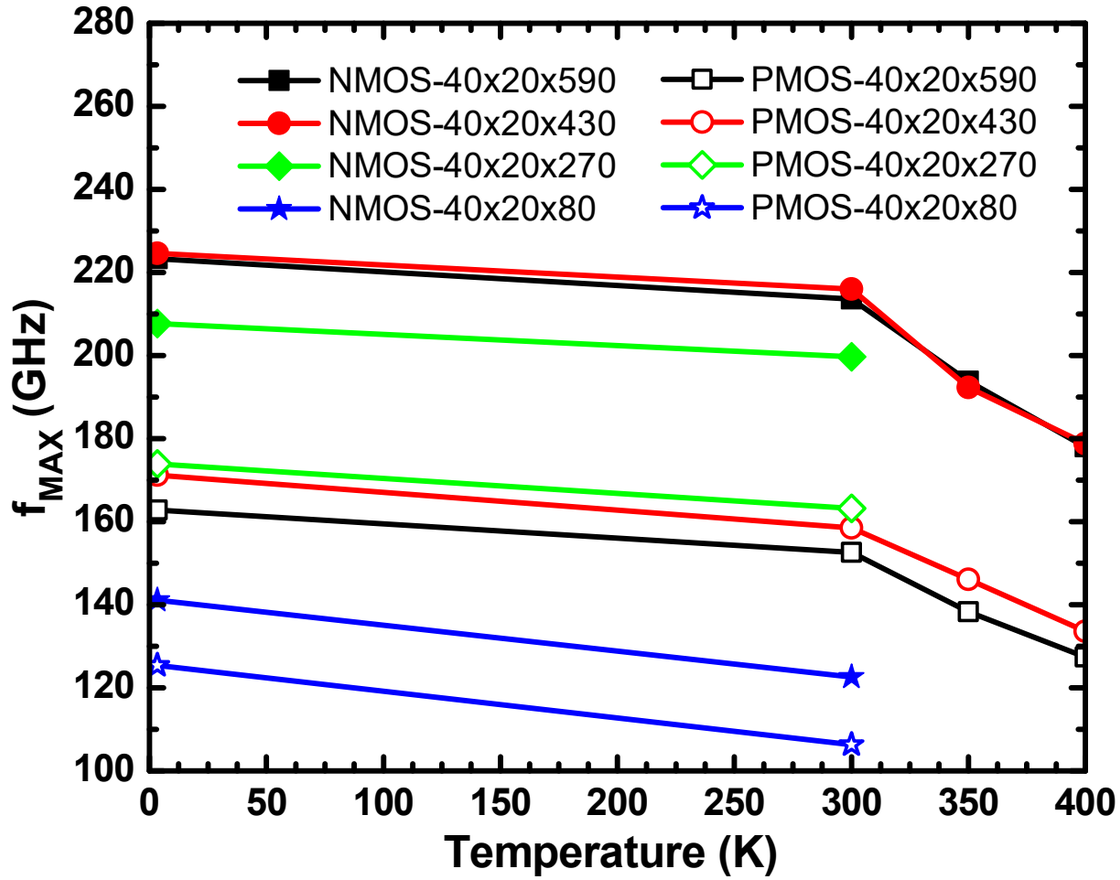



# Measured p-MOSFET $f_T, f_{MAX}$ vs. $W_f$

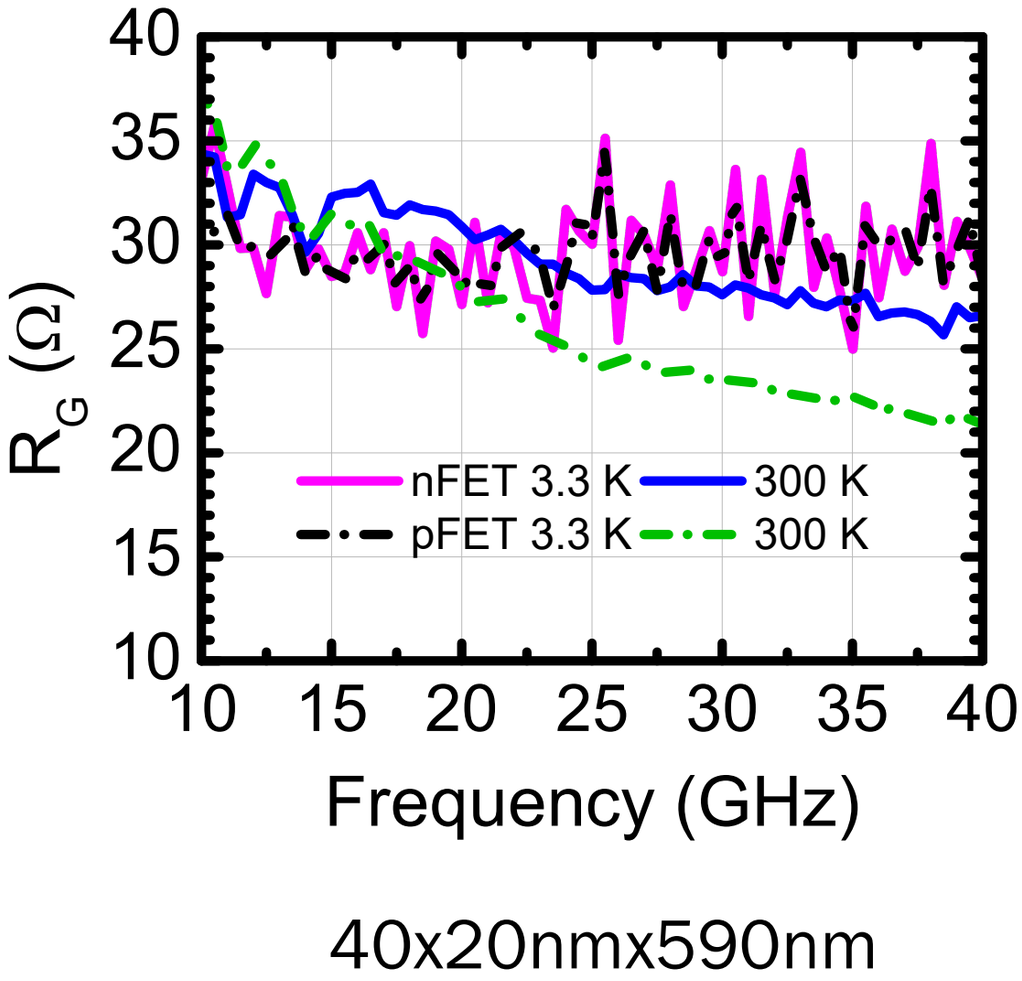


# Measured MOSFET Peak $f_T, f_{MAX}$ vs. Temperature

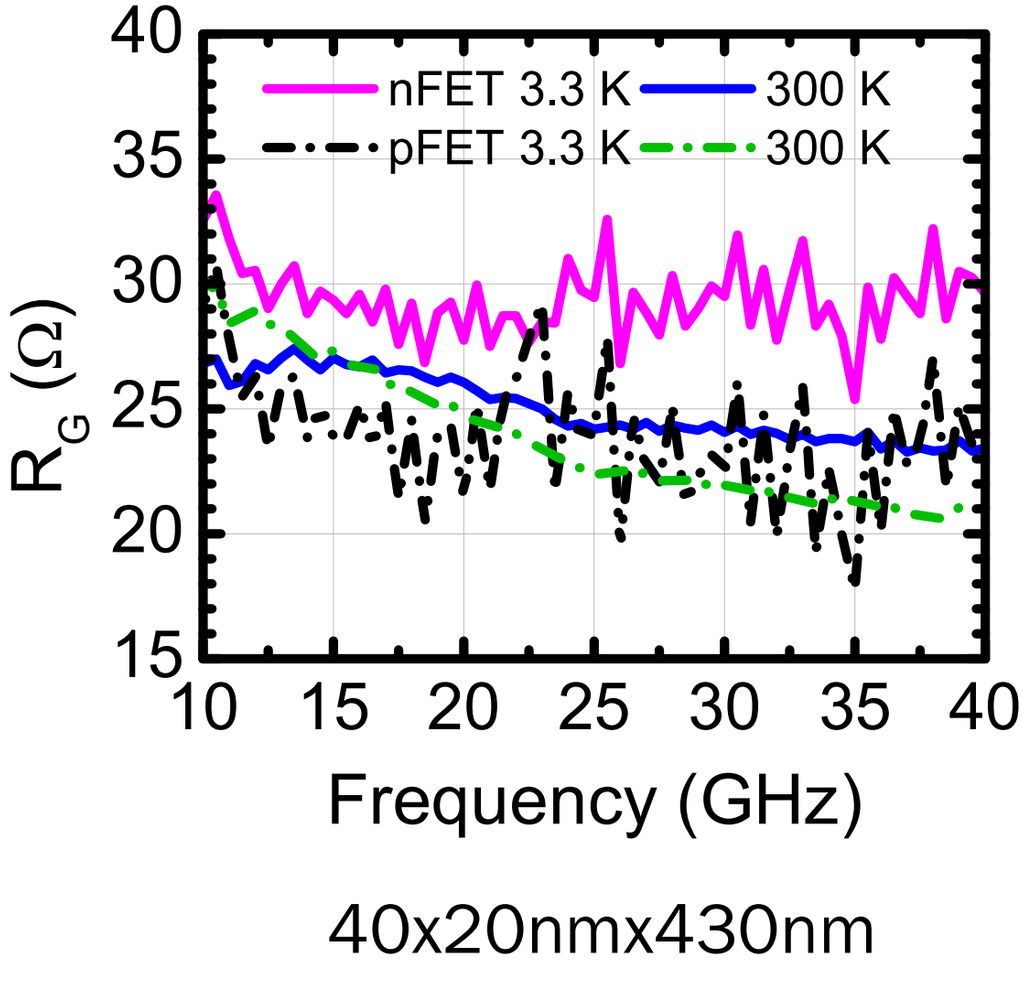


# Measured $R_G$

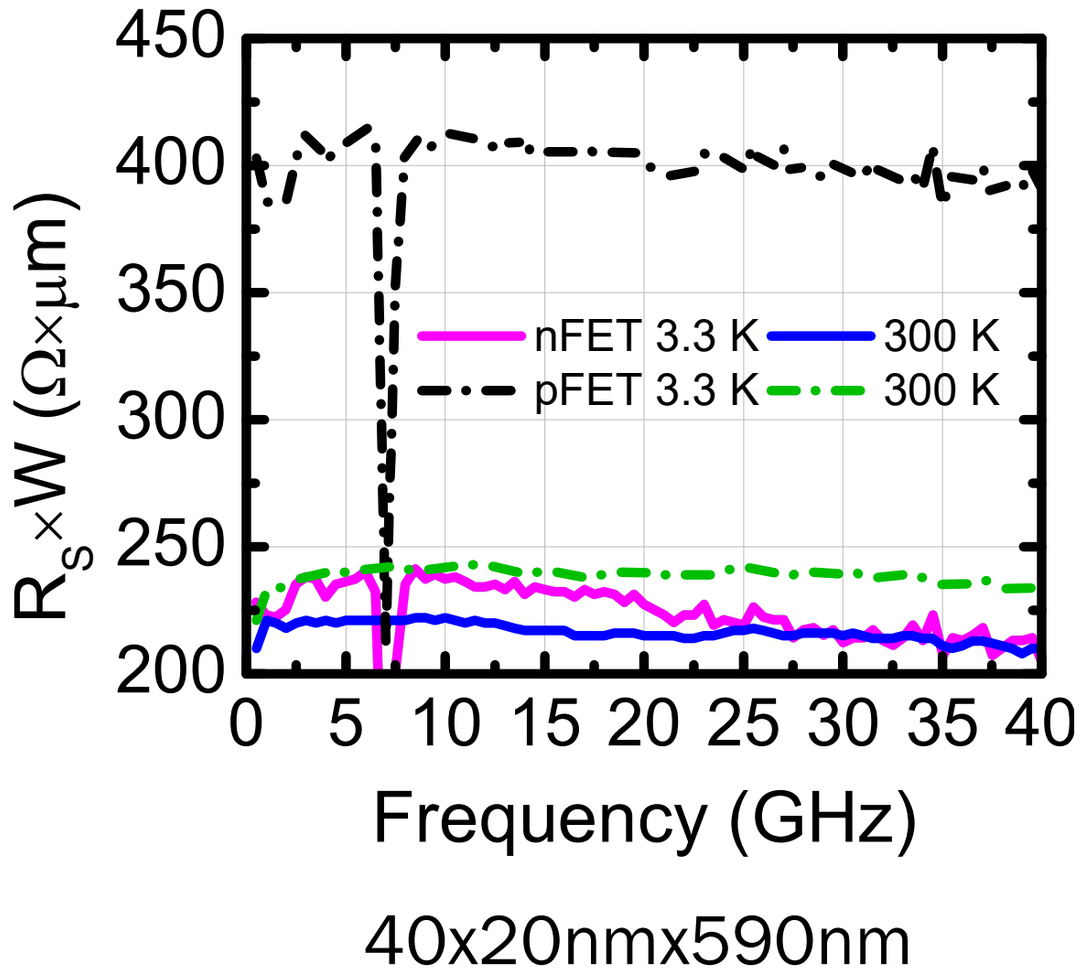



40x20nmx590nm

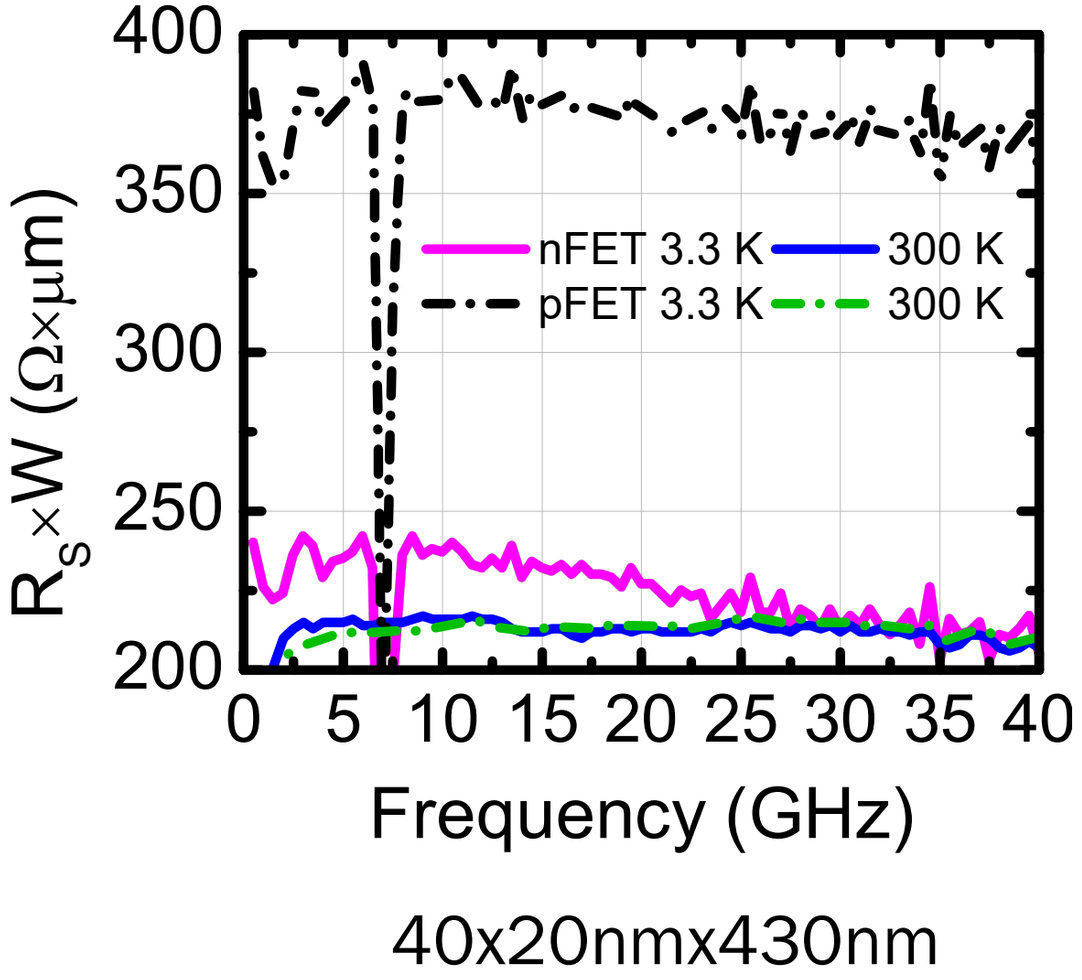



40x20nmx430nm

# Measured $R_S$

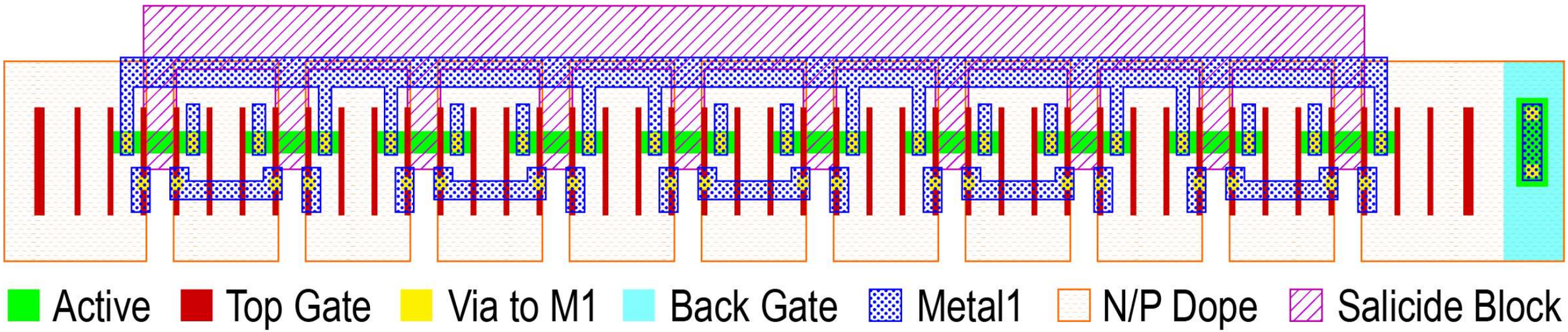



40x20nmx590nm




40x20nmx430nm

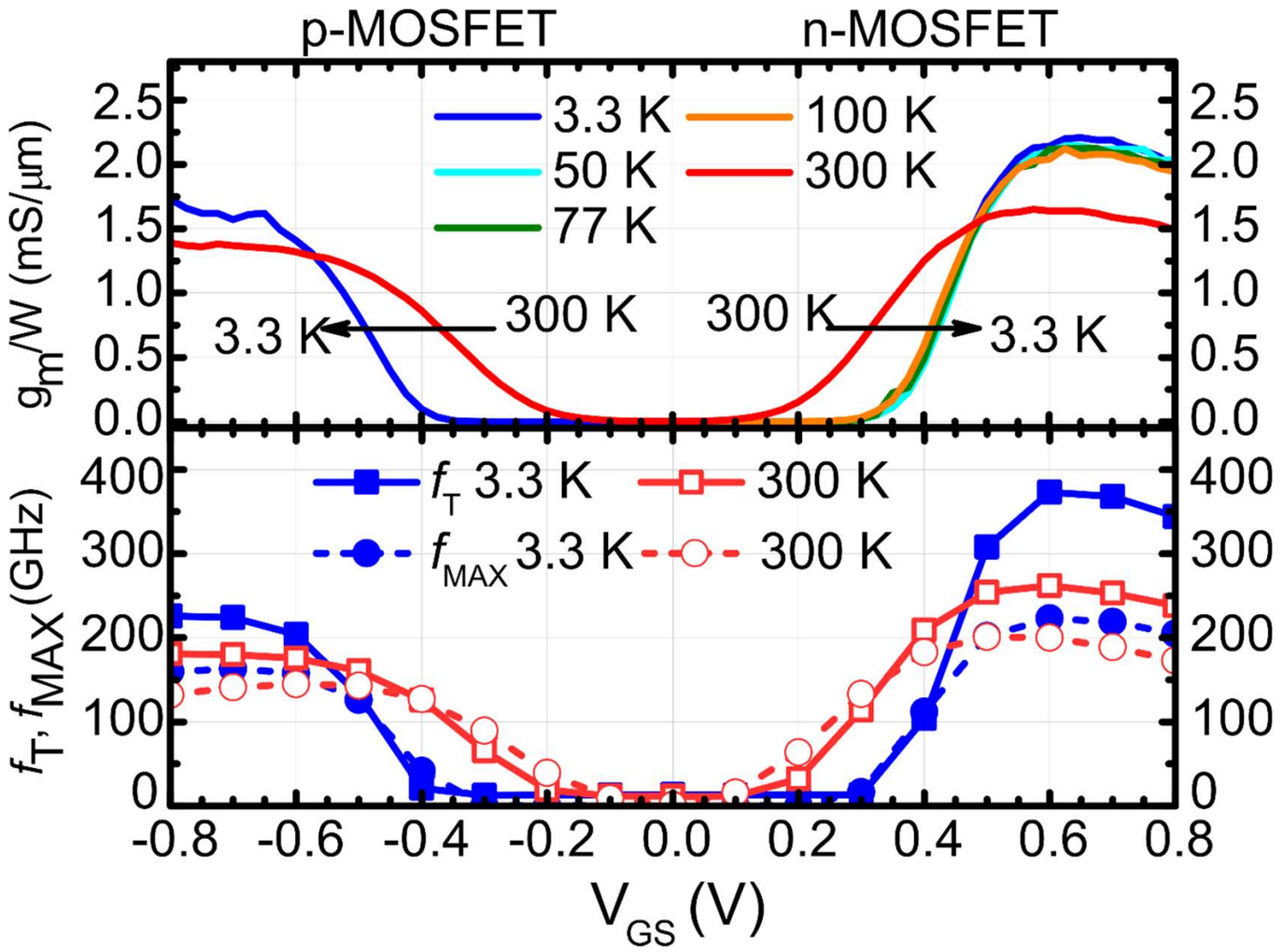
# Layout of Ten Double Quantum Dots in Parallel



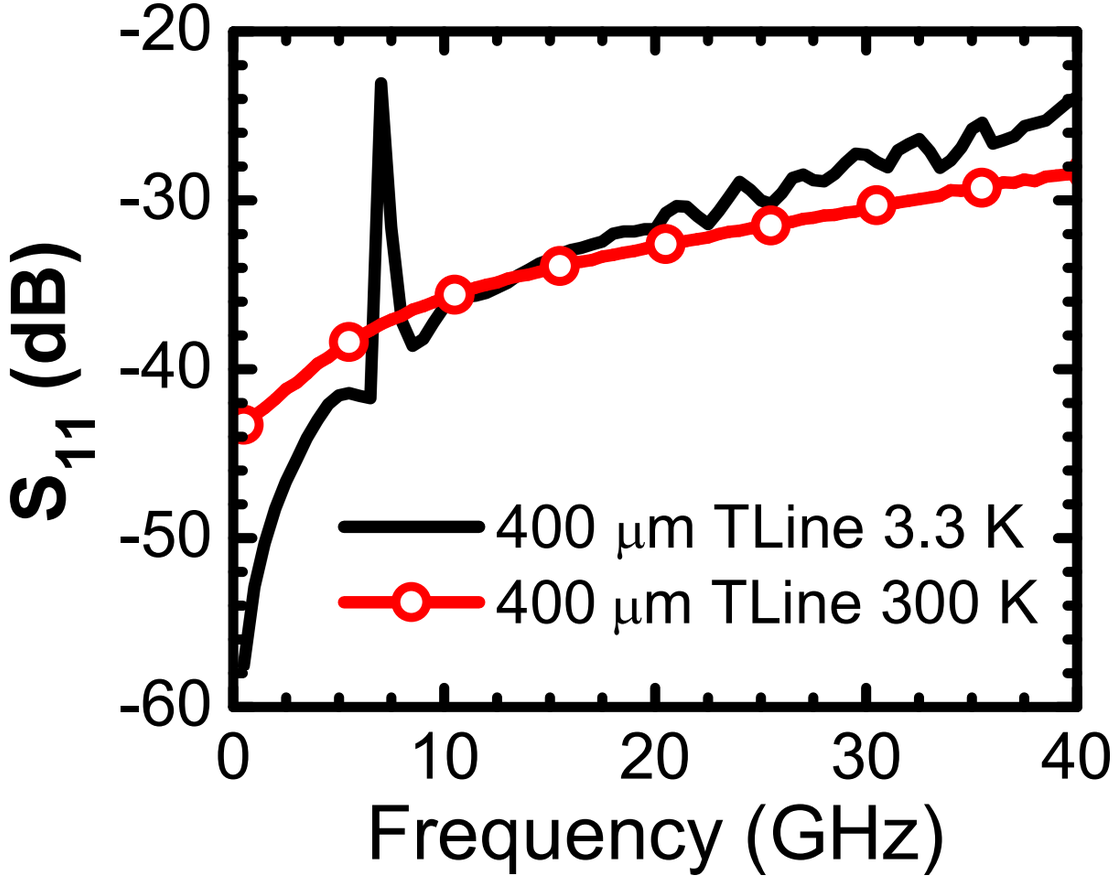

10x1x18nmx70nm cascode

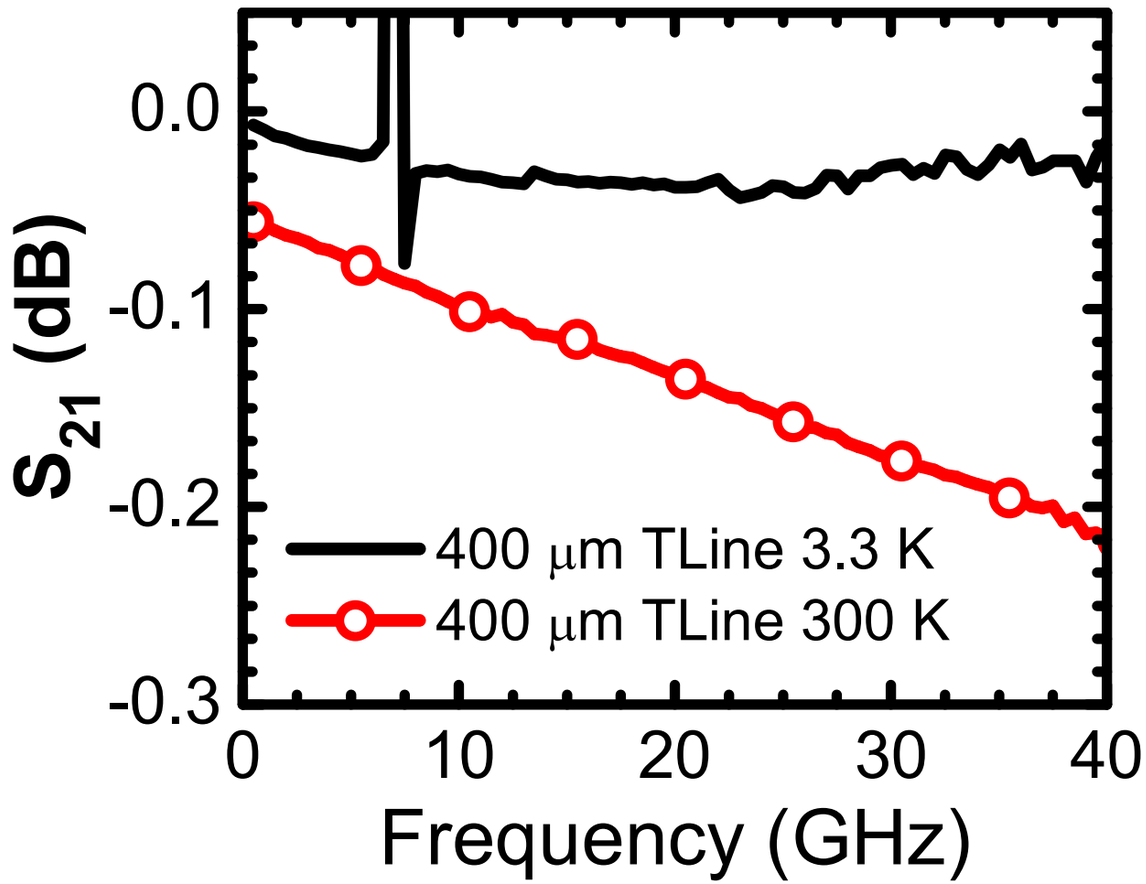
# Measured $g_m$, $f_T$, and $f_{MAX}$

- 40x20nmx590nm
- $g_m/W$, $f_T$, and $f_{MAX}$ all improve at lower temperatures
- $V_t$ changes only between 300 K and 100 K

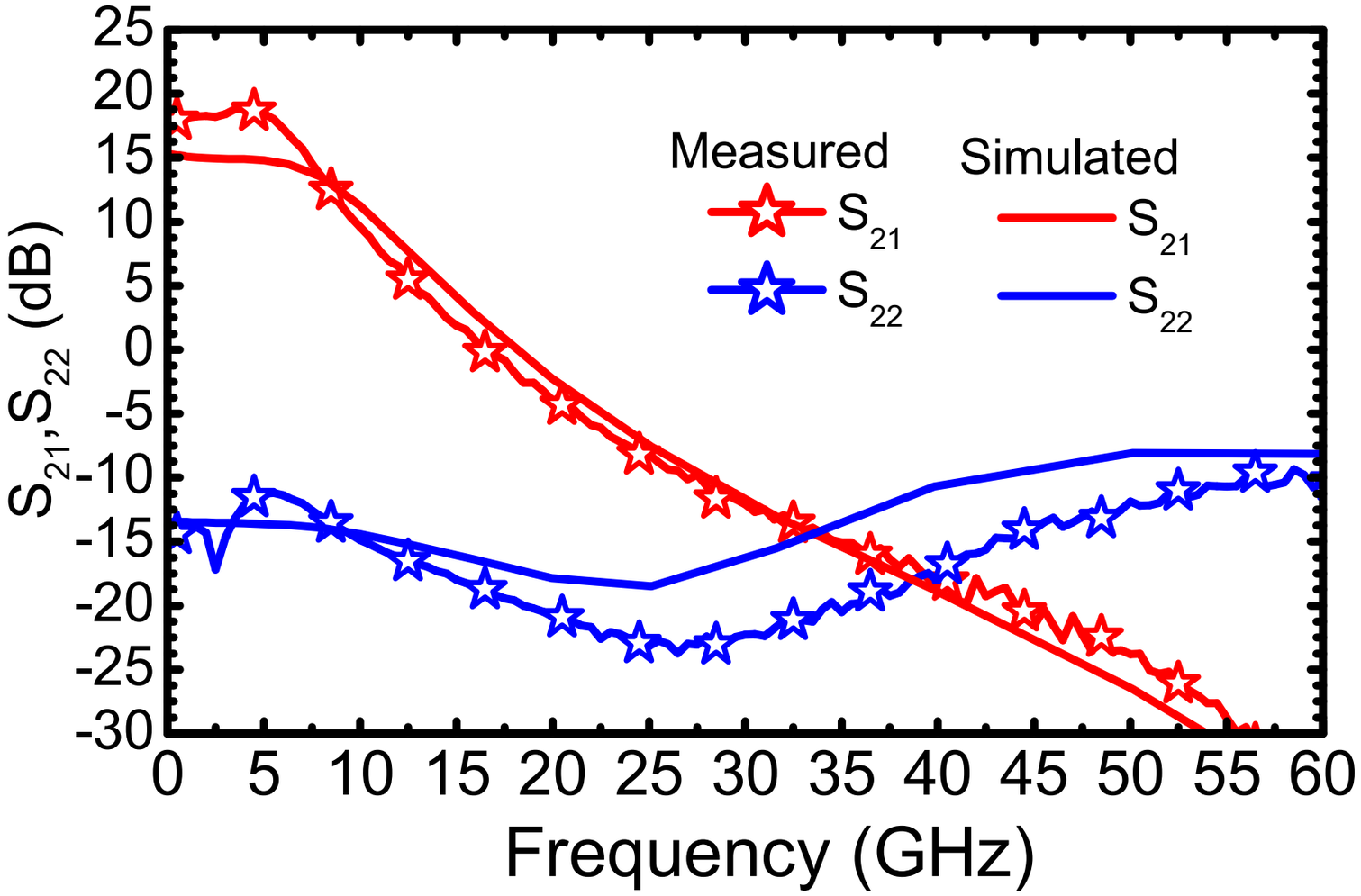


# Measured 50Ω ($5\mu m$ x $400\mu m$) Transmission Line

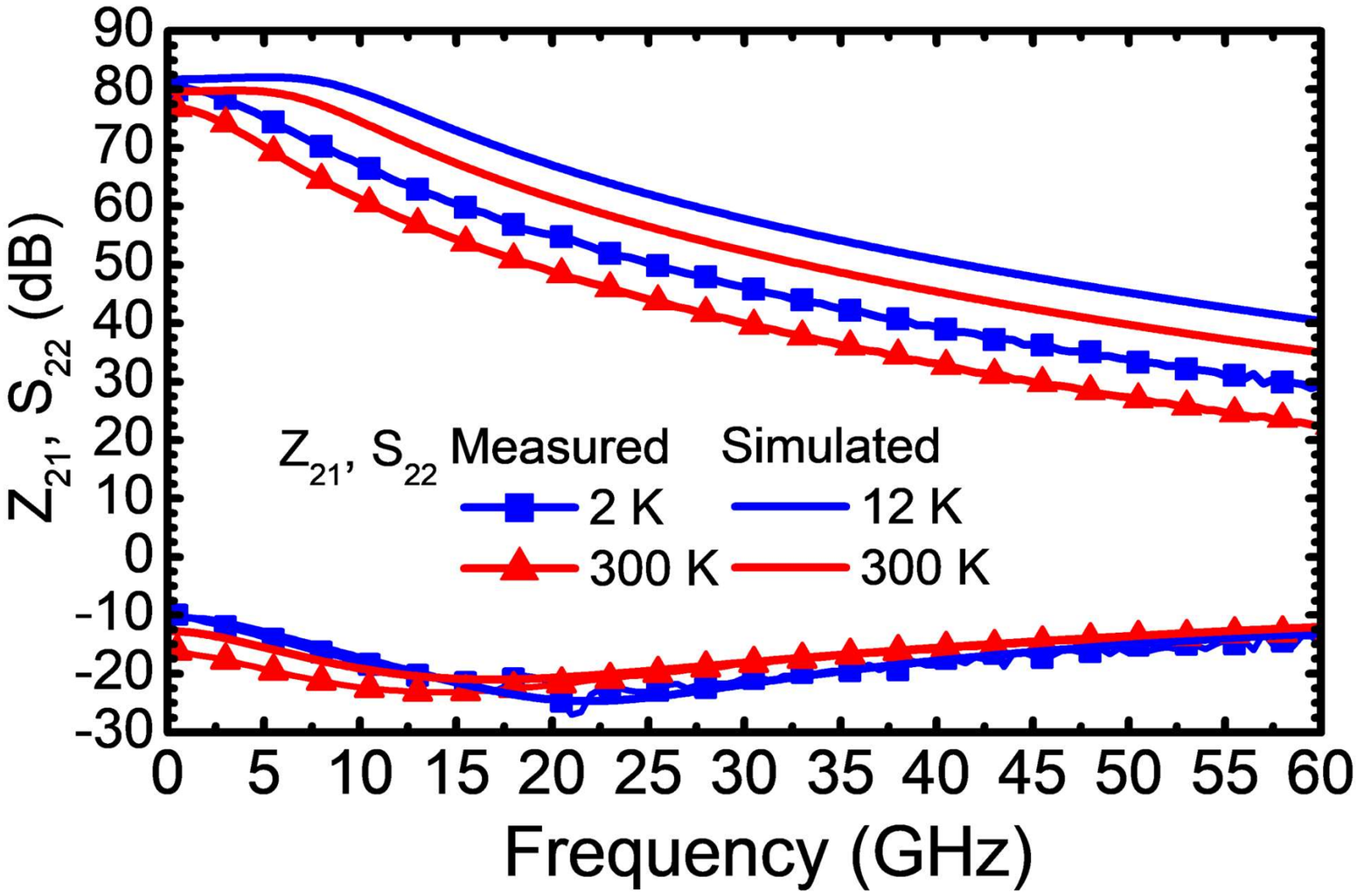


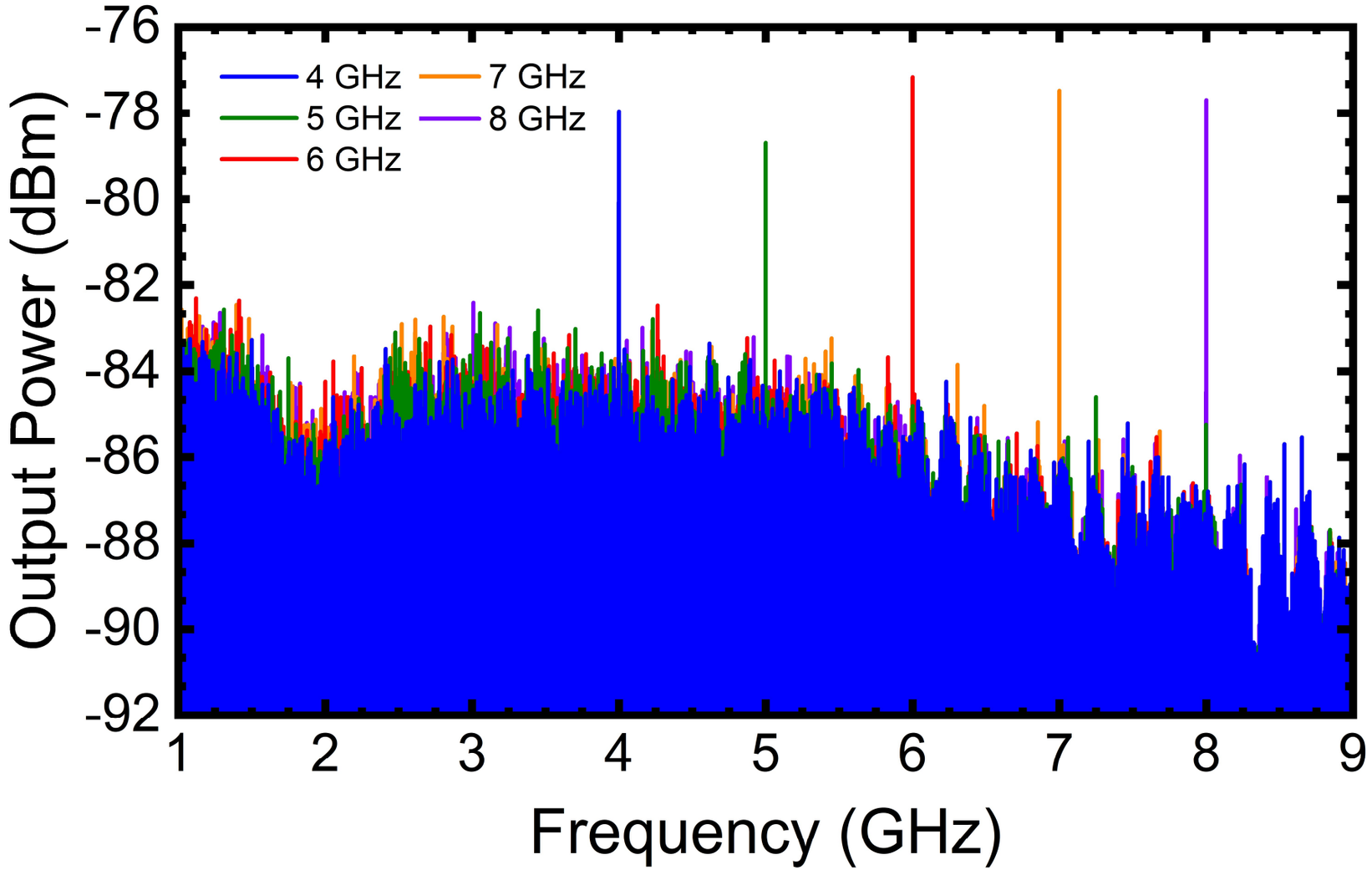
# Measured vs Simulated S-Parameters of 10xnDQD+TIA at 300 K



# Measured vs Simulated S-Parameters of 3-Stg TIA over Temp.



# Meas. 300K Output Spectrum of 1x p-DQD+TIA for Sinusoidal Inputs




RBW = 2.5 kHz