Silicon Spin Qubit Control and Readout Circuits in 22nm FDSOI CMOS

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Outline

• Silicon-based monolithic quantum processor
  — EU H2020 FET Open project IQubits
• Silicon electron/hole spin qubits
• Qubit control and readout techniques
• Qubit ICs
• Conclusions
Si-based quantum processors

• Quantum supremacy
  – Promises disruption
  – Requires highly-scalable quantum processors

• Early-stage approaches (multi-chip)
  – Quantum chip ($T < 100 \text{ mK}$)
  – Classical chip for control and readout ($T \sim 4 \text{ K}$)
  – Bulky instrumentation
  – Bulky interconnects

⇒ Not scalable
Si-based monolithic quantum processor: EU H2020 project IQubits

• Building blocks for highly-scalable quantum processor in ultra-scaled (22nm and below) FDSOI CMOS foundry techs
  — Electron/hole-spin qubits operating at $T \geq 3$ K
  — Co-integration of qubits with control and readout (RO) circuits
  — www.iqubits.eu

• Here we address the preliminary design and considerations
  — Signal generator (SG)
  — Transimpedance amplifier (TIA)

[S. Bonen et al., IEEE EDL, 2019]
Silicon electron/hole spin qubits

• Advantages
  ─ Long coherence time (isotopically-purified Si)
  ─ Compatibility with IC manufacturing techs for high-scalability

• Implementations of double quantum dots (DQDs)

[R. Maurand et al., Nature Commun., 2016]
[S. Bonen et al., IEEE EDL, 2019]

[D.M. Zajac et al., Science, 2018]
Qubit Control & RO: Magnetic field effect on spin (1/2)

- Zeeman splitting of spin states
  - Static field $B_0 \hat{z}$ lifts degeneracy
  - Energy separation $E_Z \propto B_0$
  - Spin precession about z-axis with Larmor frequency $f_L = E_Z / \hbar$
Qubit Control & RO: Magnetic field effect on spin (2/2)

- **Rabi oscillations**
  - Magnetic field $B_1(t)$ rotating at $f_L$ in xy-plane (*perturbation*)
    $\Rightarrow$ spin-up probability varies periodically with duration time
  -Freq. of oscillations: Rabi frequency ($f_R$)

- **Rotating wave approximation (RWA)**
  - Rotating field approximated by oscillating field $B(t)$
  - Requires $f_R \ll f_L$

$$B(t) = B_1(t) + B_2(t)$$
Qubit Control & RO: Spin manipulation & RO techniques

• Spin manipulation
  – Electron-spin resonance (ESR): $B(t) \propto I(t)$
  – Electric dipole-spin resonance (EDSR): $B(t) \propto V(t)$

• RO
  – Energy-selective (ERO)
  – Tunnel-rate-selective (TR-RO)
  – Spin blockade + charge sensor
  – Gate reflectometry

ES: Excited state  GS: Ground state  $\mu_{res}$: Electrochemical potential of reservoir
Monolithic qubit ICs: Performance considerations

- Qubit operation at 3 K
  - \( E_Z = k_B T \approx 0.25 \text{ meV} \)
  - \( f_L \approx 60 \text{ GHz} \)

- TIA
  - Expected tunneling currents \( \sim 10 \text{ pA} - 10 \text{ nA} \)
  - \( V_{out} \sim 1 \text{ mV} \) on 50\( \Omega \) test equipment (experimental proof)
  - Transimpedance gain: 100-140 dB\( \Omega \)

- SG
  - Voltage-controlled oscillator (VCO)
  - Phase noise (PN) affects fidelity

Fidelity: Measures how well a physical system implements a quantum gate

[S. Bonen et al., IEEE EDL, 2019; M.J. Gong et al., IEEE RFIC, 2019]
Monolithic qubit ICs: Fidelity considerations

• $\pi/2$ rotation gate

• Fidelity limited by RWA
  
  – 99.9% $\Rightarrow f_R = f_L/80 = 750 \text{ MHz}$
  
  – 99.3% $\Rightarrow f_R = f_L/5 = 12 \text{ GHz}$

• We estimated PN required for target infidelity of $125 \times 10^{-6}$

<table>
<thead>
<tr>
<th>$f_R$</th>
<th>$T_p$</th>
<th>PN$^1$</th>
<th>$\Delta t$</th>
</tr>
</thead>
<tbody>
<tr>
<td>750 MHz</td>
<td>330 ps</td>
<td>$-74 \text{ dBC/Hz}$</td>
<td>4.7 ps</td>
</tr>
<tr>
<td>12 GHz</td>
<td>20 ps</td>
<td>$-62 \text{ dBC/Hz}$</td>
<td>280 fs</td>
</tr>
</tbody>
</table>

$^1$At 1MHz frequency offset from $f_L$

$T_p$: pulse duration

$\Delta t$: uncertainty of $T_p$

[J.P.G. van Dijk et al., Physical Review Applied, 2016]
Monolithic qubit ICs: Design approach

• Cryo characterization of 22nm FDSOI CMOS down to 3.3 K
  — Peak $g_m$ of n- and p-MOSFET improves
  — Peak-$f_T$ & peak-$f_{max}$ current densities nearly constant
  — Passive devices exhibit lower losses
  — Normalized $g_m$ nearly constant below 77 K

• Circuits designed at 300 K and analyzed down to 77 K
  — Simulation convergence
  — Accurate models
  — Similar or better performance expected at 3 K

[S. Bonen et al., IEEE EDL, 2019]
[M.J. Gong et al., IEEE RFIC, 2019]
Monolithic qubit ICs: **Signal generator (SG)**

- VCO settling time \(\approx 200\) ps (too long wrt \(T_p\) of 20 ps)

- SG based on 60-GHz VCO with on/off amplitude modulation

- VCO in steady state and on/off mm-wave switches to transfer the Larmor frequency \(f_L\) carrier to the DQD control gate
Monolithic qubit ICs: PN of VCO

- PN at 1MHz frequency offset from 60GHz carrier
  - -90 dBc/Hz at T = 300 K
  - -100 dBc/Hz at T = 77 K
- VCO PN well below -62 and -74 dBc/Hz emerging from fidelity considerations
Monolithic qubit ICs: SG output signal

330ps $\pi/2$ pulse for $f_R = 750$ MHz
20ps $\pi/2$ pulse for $f_R = 12$ GHz

- Rise and fall times of $V_C$ set equal to $\Delta t/2$
- Output voltage ($V_{SG}$) of SG generated correctly
- Pulses are slightly longer due to switch non-idealities
Monolithic qubit ICs: Transimpedance amplifier (TIA)

- Circuit topology
  - Mutuated from [M.J. Gong et al., IEEE RFIC, 2019]
  - But here only two inductors of 400 pH ⇒ Higher scalability
- Transistors biased at peak-$f_{\text{max}}$ current density
- Input-stage MOSFETs sized for minimum input-referred noise-current spectral density ($i_{nTIA}$)
Monolithic qubit ICs: TIA performance

- Simulation results at 300 K (black) and 77 K (blue)

<table>
<thead>
<tr>
<th>$T$ (K)</th>
<th>$P_C$ (mW)</th>
<th>$Z_{21}$ (dBΩ)</th>
<th>$BW$ (GHz)</th>
<th>$i_{nTIA}$ (pA/√Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>4.9</td>
<td>108</td>
<td>18</td>
<td>0.89</td>
</tr>
<tr>
<td>77</td>
<td>5.5</td>
<td>111</td>
<td>25</td>
<td>0.44</td>
</tr>
</tbody>
</table>
Conclusions

• Summary of techniques for control and RO of electron/hole spin qubits
• Preliminary design of SG and TIA in 22nm FDSOI CMOS tech
  • SG
    — 60GHz sinusoidal pulses for $\pi/2$ rotation gates with $f_R$ up to 12 GHz and min $T_p$ of 20 ps
  • TIA
    — $Z_{21}$ of 108 dBΩ, 3dB BW of 18 GHz, $i_{nTIA}$ of 0.89 pA/√Hz at 300 K
• Future works
  — Physical implementation
  — Experimental verifications down to 3 K
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